EUROPEAN
COMMISSION

Brussels, 3.6.2026
SWD(2026) 504 final

PART 3/3

COMMISSION STAFF WORKING DOCUMENT

IMPACT ASSESSMENT REPORT

Accompanying the document

Proposal for a Regulation of the European Parliament and of the Council

on a framework of measures for strengthening Europe's semiconductor ecosystem repealing Regulation (EU) 2023/1782 (Chips Act 2.0)

{COM(2026) 504 final} - {SEC(2026) 504 final} - {SWD(2026) 505 final}

Table of contents

1. INTRODUCTION 1
   1.1. Purpose and scope of the evaluation/fitness check 1
   1.2. Methodology 2
2. WHAT WAS THE EXPECTED OUTCOME OF THE INTERVENTION? 4
   2.1. Description of the intervention and its objectives 4
      2.1.1. Context of the intervention 5
      2.1.2. Strategic Objectives behind the Chips Act 6
      2.1.3. Activities and pillars 7
      2.1.4. Inputs to the Chips Act 12
      2.1.5. Expected outputs, results, and impacts 12
   2.2. Points of comparison 13
3. HOW HAS THE SITUATION EVOLVED OVER THE EVALUATION PERIOD? 14
   3.1. The implementation of the Chips Act 14
      3.1.1. Pillar I 14
      3.1.2. Pillar II 19
      3.1.3. Pillar III 21
   3.2. Unexpected or unintended changes 25
4. EVALUATION FINDINGS 27
   4.1. To what extent was the intervention successful and why? 27
      4.1.1. Effectiveness 27
      4.1.2. Efficiency 39
      4.1.3. Coherence 44
   4.2. How did the EU intervention make a difference and to whom? 46
      4.2.1. EU added value 46
   4.3. Is the intervention still relevant? 48
      4.3.1. Relevance 48
5. WHAT ARE THE CONCLUSIONS AND LESSONS LEARNED? 53
   5.1. Conclusions 53
   5.2. Lessons learned 54

ANNEX I – EVALUATION MATRIX 56
ANNEX II – MAIN POINTS OF COMPARISON 71
ANNEX III – OVERVIEW OF BENEFITS AND COSTS 73

1. INTRODUCTION

1.1. Purpose and scope of the evaluation/fitness check

Adopted in September 2023, regulation (EU) 2023/1781 establishing a framework of measures for strengthening Europe's semiconductor ecosystem ("**Chips Act**" or "the Regulation") represents a cornerstone initiative to reinforce the Union's semiconductor ecosystem by reducing dependencies, enhancing digital sovereignty, stimulating investment, strengthening the capabilities, security, adaptability and resilience of the Union's semiconductor supply chain, and increasing cooperation in the domain among the Member States, the Commission, and international strategic partners.

Since then, the rapid digital transformation of Europe's economy – driven by the expansion of artificial intelligence (AI), cloud and edge computing, and connected devices – has intensified the demand for secure, high-performance semiconductors and exposed new vulnerabilities in global supply chains. Recent geopolitical tensions have underscored the strategic importance of ensuring Europe's capacity to design and produce advanced semiconductors domestically, positioning semiconductors as a strategic industry for other strategic (user) industries. In this context, the Chips Act has become a central pillar of the EU's strategy to enhance technological sovereignty, resilience, and security.

In accordance with Article 40 of the Chips Act Regulation, the European Commission (hereafter – the Commission) must submit a first report on the evaluation and review of the Regulation to the European Parliament and to the Council by 20 September 2026. Therefore, the purpose of the evaluation was to produce a **critical, unbiased, and evidence-based judgement of the progress of the Chips Act and its ability to strengthen the Union's semiconductor ecosystem**.

In accordance with the Better Regulation Guidelines, the evaluation aims to measure to what extent the legislation is **effective, efficient, relevant, coherent, and brings clear EU added value**. It covers the **three pillars of the Chips Act** (The Chips for Europe Initiative, security of supply, and monitoring and crisis response), and cross-pillar elements.

The evaluation examines **the impact of the Chips Act** on the economy, governance and social factors, alongside the impact assessment for this initiative (where an in-depth impact assessment of each policy option is provided). It also identifies and quantifies **the costs and benefits of the Chips Act** under each Pillar. Finally, the evaluation outlines **the lessons learned** from its implementation and highlights persisting and emerging issues affecting the Regulation's functioning.

The evaluation focuses on the period starting from the entry into force of the Chips Act on **21 September 2023 until end of November 2025** ([1]). Depending on the results from the evaluation of the functioning of the Chips Act and an impact assessment, the Commission may propose measures aimed at possible adaptations that ensure the Chips Act remains fit for purpose in light of changing market, technological, and geopolitical realities.

([1]) November 2025 was set as the cut-off date since this was the last time data collection was conducted for the report.

This staff working document describes the evaluation, how it was carried out, and its main findings. The report, structured in alignment with the Better Regulation Guidelines of the Commission, covers the following chapters and annexes:

- Section 1 introduces the evaluation and its methods;
- Section 2 presents the background to the intervention and its expected outcomes;
- Section 3 summarises the state of play in implementing the programme;
- Section 4 provides answers to the evaluation questions;
- Section 5 presents the evaluation results, conclusions and lessons learned;
- Annex I: evaluation matrix
- Annex II: main points of comparison
- Annex III: cost-benefit analysis

1.2. Methodology

The report draws on **sound evaluation methods** and **evidence from across the EU Member States**, gathered through stakeholder consultation, case studies, cost-benefit analysis, and desk research, as well as positions and findings from the European Parliament, the Council, and the European Semiconductor Board (ESB). On 5 September 2025, the Commission launched an **open public consultation** and a **call for evidence** on the evaluation and review of the Chips Act, with a feedback period of 12 weeks. The open public consultation was **complemented by an external study** ([2]), the contractors of which carried out targeted surveys and interviews, organised dedicated workshops, and provided input to the evaluation and drafting of the impact assessment. In addition, the Commission organised a number of targeted consultations and workshops with different types of stakeholders (e.g., Member States of the Chips JU's Public Authorities Board, industry associations, companies, RTOs, etc.) in the second half of 2025.

The consultation activities aimed at collecting the views, positions, and findings of:

- Industry stakeholders across the semiconductor value chain (IDMs, fabless companies, design houses, equipment manufacturers, suppliers);
- Industrial users of semiconductors in sectors such as automotive, telecom, healthcare, energy, industrial robotics and manufacturing, defence, and security;
- EU Member States represented in the European Semiconductor Board (ESB);
- The European Parliament ([3]);
- The Council of the European Union ([4]);
- National competent authorities, including semiconductor-relevant authorities;
- EU bodies such as the Chips JU Office, EISMEA, EIB, and EIF;
- Start-ups, SMEs, and scale-ups;
- Research and Technology Organisations, academia, and scientific associations;

([2]) An external study carried out by PPMI and partners supported the Commission during the evaluation and impact assessment process. The study kicked off in September 2025 and should be finalised by April 2026. The final report of the study was not yet submitted at the time of writing this report.

([3]) European Parliament resolution on European technological sovereignty and digital infrastructure (2025/2007(INI)), 11 June 2025.

([4]) Declaration of the Semicon Coalition calling for a revised EU Chips Act in order to strengthen and revitalize Europe's position in the global semiconductor industry, 29 September 2025.

- Trade and industry associations;
- Investors, including venture capital and private equity;
- NGOs, think tanks, and other civil society organisations;
- Independent experts and consultants.

Table 1. Overview of consultation activities

Activity type	Method	Number
Workshops	Thematic workshops	17 workshops
Public Consultations	Open Public Consultation (OPC)	103 replies
	Call for Evidence (CfE)	209 replies
Targeted surveys	National authorities survey	24 responses
	RTO & design survey	17 responses
	Supply chain survey	16 responses
	Industry users survey	7 responses
	Total surveys	64 responses
Interviews	Expert interviews	17 interviews

Overall, the evaluation of the Chips Act provides robust evaluation findings built on the analysis of quantitative and qualitative data collected through desk research, stakeholder consultation activities and case studies. However, a few limitations of the evaluation, while rather marginal and mitigated by the evaluation team as explained below, should be mentioned.

First, the evaluation mostly considers **the achievement of outputs and short-term outcomes**, since the Chips Act has only operated for a few years, and some initiatives are still in the early phase of implementation. This challenge was mitigated by combining the stakeholders' positions and opinions on achieving the intended results and impacts with the assessment of impacts of the Chips Act 2.0 in the impact assessment report.

Second, because initial stakeholder participation in the OPC and survey was somewhat low**, additional targeted consultations were incorporated into the consultation plan**. These included thematic workshops with various stakeholder groups. Following the increase in responses to the OPC and survey, the final results of consultation activities reflect a well-balanced mix of quantitative and qualitative, as well as retrospective and prospective insights.

To ensure terminological consistency and clarity throughout this report, a comprehensive **glossary** of key terms has been developed based on official EU policy documents, specifically Regulation (EU) 2023/1781 (the Chips Act) ([5]). This glossary serves as the definitional framework for analysing Europe's semiconductor strategy and its implications for technological sovereignty. All terms used in the analysis adhere to these official definitions unless otherwise specified. The glossary is found under the Impact Assessment.

([5]) https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32023R1781.

2. WHAT WAS THE EXPECTED OUTCOME OF THE INTERVENTION?

2.1. Description of the intervention and its objectives

This section presents the **intervention logic** underpinning the Chips Act, and the core problems it aimed to tackle. The intervention logic highlights the linkages between the needs, activities and expected impacts. It consists of a logical chain, whose success depends *inter alia* on the timing of the implemented activities, level of support provided by industry, the Member States, and the Union, and the role of external actors. The final impacts are largely beyond the direct control of the Commission.

Figure 1. Intervention logic

The causal chain includes the following specific elements:

- **External factors:** overarching global conditions that influence the policy environment;
- **Needs (or problems)** addressed by the Chips Act;
- **Stakeholders:** actors with an interest in or affected by the policy;
- **Strategic objectives** of the Chips Act;
- Eligible **actions** of the Chips Act (organised in pillars);
- **Inputs**: the Chips Act's financial and administrative resources;
- **Outputs**: tangible and measurable products and services of different types directly produced by implementing the activities of the Chips Act pillars;
- **Results**: short- and medium-term results, in terms of behaviour or practice of the target group(s), organisational or policy changes;
- **Impacts**: long-term institutional and policy changes that the programme's implementation is expected to contribute to.

The elements of the intervention logic listed above link to **the evaluation criteria in focus** in the evaluation (effectiveness, efficiency, relevance, coherence and EU-added value). For instance, while effectiveness is concerned with the achievement of objectives, expected outputs, outcomes and impacts, relevance is concerned with the match between objectives, inputs and actions with the needs of the stakeholders. More information on the methods underpinning the data collection and analysis of the evaluation can be found in the Synopsis Report.

2.1.1. Context of the intervention

The Chips Act constitutes **the EU's strategic response to critical vulnerabilities** exposed in the global semiconductor supply chain as a result of the COVID-19 pandemic and intensifying subsidy-driven competition with third countries ([6]). The semiconductor sector faced a series of shocks due to the COVID19-related shutdowns of manufacturing facilities, workforce disruptions, and shipping delays since early 2020. A shortage of semiconductors in the EU disrupted industrial activity, with the automotive sector experiencing production cuts exceeding 30%, and Germany's car output falling by 34% in 2021 compared to 2019, reaching levels last seen in 1975 ([7]). The crisis extended beyond automotive manufacturing, affecting healthcare equipment, renewable energy installations, and defence systems, revealing the risks of Europe's dependency on external suppliers concentrated primarily in East Asia ([8]). The semiconductor market, valued at over USD 555 billion in 2021 and projected to exceed USD 1.3 trillion by 2030 ([9]), had become central to economic competitiveness and national security. Europe's strategic position was becoming precarious: **companies in the EU accounted for only 9% of global semiconductor production by headquarter location**, although the region

([6]) SWD(2022) 147, *A Chips Act for Europe*, European Commission, Staff Working Document, Brussels, 11 May 2022.

([7]) Verband der Automobilindustrie, https://en.vda.de/en/press/press-releases/220105_German-car-market-2021--recovery-slowed-down.html.

([8]) Iggo, C., and T. Riley, 'Why Semiconductors Have Become a Geopolitical Issue – and What It Means for Investors', AXA IM Corporate, 2022. https://www.axa-im.com/investment-institute/investment-themes/technology/why-semiconductors-have-become-geopolitical-issue-and-what-it-means-investors.

([9]) SEMI "Why AI will propel semiconductor market to $1 trillion and achieve 1.0 nm by 2030", November 20, 2025 https://www.semi.org/sites/semi.org/files/2024-11/MS-SEMIWEB11.2024.pdf.

represented 20% of the worldwide end-user market, resulting in a EUR 19.5 billion trade deficit in 2021 ([10]).

The EU determined that **decisive, coordinated intervention was essential** to address structural dependencies in its semiconductor ecosystem and to support the industry. Member States required significant capacity to strengthen innovation systems, attract investments, and reduce external dependencies that threatened both economic resilience and technological sovereignty ([11]). Meanwhile, **coordinated action at EU level was necessary to address Europe's declining competitive position in semiconductors**, as other major economies deployed unprecedented state subsidies to strengthen domestic manufacturing capabilities. Previous crises had shown that concentrated semiconductor production in a few regions created vulnerabilities across multiple sectors ([12]). Europe's **global value chain market share** (9.9% in 2019, 9.3% in 2020, 8.9% in 2021) ([13]) was insufficient to guarantee supply security. Without substantial investments in research, manufacturing capacity, and crisis response mechanisms, Europe would remain structurally vulnerable. The Chips Act emerged during a period of **strong focus on green and digital transitions**, and amid growing European consensus on the need to strengthen the region's **economic competitiveness and reverse declining industrial capacity**. The September 2024 Draghi report would later articulate these concerns comprehensively, calling for urgent industrial renewal ([14]).

2.1.2. Strategic Objectives behind the Chips Act

Given the **central role that chips play in the digital economy**, their geopolitical dimension and the current strong concentration in production capacity, the Union had to urgently reinforce its semiconductor ecosystem, increasing its resilience as well as security of supply and reducing its external dependencies. Europe would have to mobilise an unprecedented level of investment given the high positive spill-over effects the sector has across the economy and many areas of public interest. Europe would have to mobilise all its talents and assets. The overall level of policy-driven investment in support of the EU Chips Act was estimated to be in excess of **EUR 43 billion** up to 2030([15]).

While Europe was leading in research with important organisations across the continent, it would have to close the "gap from the lab to the fab" by leveraging its strengths in (i) equipment and materials, (ii) systems solutions and systems integration, (iii) strong presence in high-growth market segments like automotive, medtech, communications, energy and machinery, and (iv) research and academic excellence, where technology

---

([10]) European Commission, ISDB, Comext, cited in the Staff Working Document (see footnote 6) under Figure 16.

([11]) SWD(2022) 147, *A Chips Act for Europe*, European Commission, Staff Working Document, Brussels, 11 May 2022.

([12]) Ragonnaud, G., *The EU Chips Act: Securing Europe's Supply of Semiconductors*, European Parliamentary Research Service, PE 733.596, European Parliament, June 2023.

([13]) Contract: CNECT/2022/MVP/0084, *Semiconductors market data by feature size, sector and region*, IDC, September 2025.

([14]) Draghi, M., *The future of European competitiveness: A competitiveness strategy for Europe*. Brussels, 2024.

([15]) COM(2022) 45, *A Chips Act for Europe*, Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions. Brussels, 8 February 2022.

capacities should be further reinforced. Successful outcomes crucially depend on joint efforts and close collaboration of all sides – industry along the value chain, public sector and research organisations ([16]).

To fulfil the above, the Chips Act strategy was articulated around the following five strategic objectives:

- First (Strategic Objective 1 (SO1)), Europe should **strengthen its research and technology leadership**. This was an imperative to preserve Europe's current assets in several break-through technologies, including in equipment manufacturing and advanced materials, needed to build next-generation production facilities serving all its sectors.
- Second (SO2), **Europe must strengthen its capacity to innovate in the design, manufacturing and packaging of advanced, energy-efficient and secure chips**, and translate these innovations into manufactured products. This was key to ensuring long-term supply for industry and the public sector and to driving wider economic innovation. Achieving this would require major investment in pilot lines and in advanced design, testing and experimentation facilities. These world-class pilot lines—open to all supply-chain actors on non-discriminatory terms—would position Europe as a strong global partner and support deeper international cooperation.
- Third (SO3), **Europe must establish a framework to substantially expand its chip production capacity by 2030**. With the market expected to double, Europe must quadruple output to meet its goals. This was not only about volume: Europe must also be able to produce advanced chips, meet user needs, enter markets where it was absent, and account for environmental impacts. Strengthening security of supply, especially for public-safety-critical sectors, would be essential. Achieving this would require attracting major investments (both EU and non-EU) into production facilities and creating the right conditions for large-scale private investment.
- Fourth (SO4), Europe should **address the acute skills shortage, attract new talent and support the emergence of a skilled workforce**, as shortages were limiting efforts aimed at strengthening the ecosystem.
- Fifth (SO5), Europe should **develop an in-depth understanding of global semiconductor supply chains** to monitor its functioning, understand future trends, anticipate disruptions, build international partnerships based on more balanced capabilities and mutual interest, react in time to prevent international supply chains from breaking down, and enable the EU to take appropriate measures when necessary.

2.1.3. Activities and pillars

To achieve the Strategic Objectives, the Regulation established **a comprehensive framework built on three pillars:**

- The first pillar, **the Chips for Europe Initiative**, is about **Europe's research policy** in the semiconductor field. It focuses on capacity building and research and innovation support to strengthen design, manufacturing and systems integration capabilities across the Union's semiconductor value chain.

([16]) Ibidem

- The second pillar is about developing a European **industrial policy** in semiconductors aiming for **security of supply and resilience**, which would attract investments by providing criteria to recognise and support integrated production facilities (IPFs) and open EU foundries (OEFs) that are first-of-a-kind (FoaK) facilities.
- The third pillar is about **crisis management**. It establishes a coordination mechanism between the Member States and the Commission for **monitoring and crisis response**, enabling the Union to map and monitor the semiconductor sector while preparing for and responding to potential chip shortages.

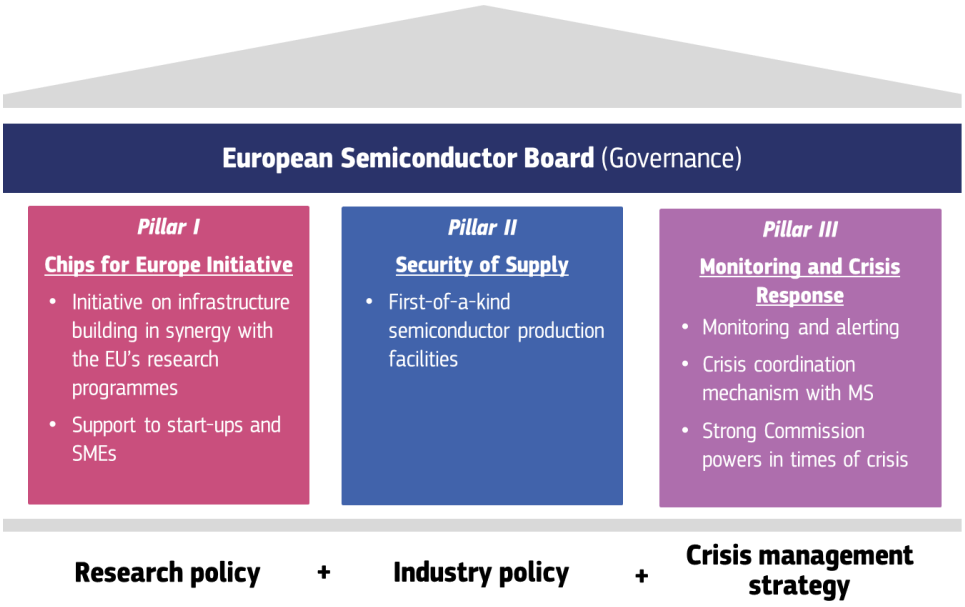

Figure 2. Pillars of the Chips Act

2.1.3.1. Pillar I - The Chips for Europe Initiative

The first pillar, the Chips for Europe Initiative, plays a central role in building technological capacity. While contributing to the green and digital transitions, the Initiative aims to **achieve capacity-building and support related research and innovation**. The first pillar provides the tools and instruments to address the above-mentioned Strategic Objectives 1), 2) and 4).

The capacities developed under the Chips for Europe Initiative are designed to strengthen the maturity, connectivity and resilience of the European semiconductor ecosystem and to accelerate the transfer of innovation from research to industrial deployment. State-of-the-art **pilot lines** offer shared, industrial-scale environments where new technologies can be tested, validated and prepared for production, reducing the risks associated with scaling up research results, and supporting the transition from laboratory prototypes to manufacturing-ready processes. The **design platform** focuses on reinforcing Europe's capabilities in chip design, helping to reduce dependence on non-EU tools and enabling companies (particularly SMEs and start-ups) to develop more complex and system-level products. **Competence centres** act as entry points to expertise, training and technology support, anchoring knowledge in regional ecosystems, and facilitating access to infrastructure and skills across Member States. **Quantum chip pilots** prepare Europe for emerging computing and sensing technologies by creating pathways from frontier

research to manufacturable components, while the **Chips Fund** complements these infrastructures by improving access to risk finance and scale-up capital. The rationale and intended outcomes of each component of the Initiative are set out below.

Pilot lines

The Initiative supports the enhancement of existing and development of new advanced **pilot lines** on cutting-edge and next-generation semiconductor technologies for industry to **test, experiment and validate** semiconductor technologies and system design concepts at high technology readiness levels.

The pilot line technology areas were chosen to close Europe's most critical semiconductor gaps while building on existing strengths, securing long-term competitiveness, security of supply, and industrial resilience. **Sub-2 nm logic** was prioritised to anchor Europe in the advanced nodes that power AI, HPC, data centres and next-generation communications, domains where Europe previously lacked manufacturing capacity and risked technological lock-out. **FD-SOI** capitalises on a field where Europe already leads, delivering low-power, high-reliability chips for automotive, mobility, industrial automation, and Internet of Things without depending on the most advanced nodes. **Advanced packaging and heterogeneous integration** were selected because future performance gains hinge on system-level integration; Europe faced a strategic weakness in packaging but also a major opportunity to lead in chiplets, 3D stacking, and the co-integration of logic, memory, sensing, and connectivity. **Wide-bandgap materials** (such as SiC and GaN) match Europe's strengths in power electronics and are vital for the energy transition, electric mobility, renewable infrastructure, and high-efficiency industrial systems. **Photonic integrated circuits** were included because of their growing importance for high-bandwidth, low-power data transmission, sensing and advanced computing architectures in telecoms and data centres. Together, these technologies will shape future industrial competitiveness, sustainability, and digital sovereignty, while reducing Europe's exposure to strategic dependencies.

Design platform

The Initiative sought to **strengthen Europe's design capacity** by creating a Union-wide virtual design platform connecting design houses, start-ups, SMEs, IP and tool suppliers, and research organisations. This shared environment would enable virtual prototyping and coordinated technology development.

Design is where around half of semiconductor value added and R&D spending occurs. Fabless firms dominate this phase, growing 2.7× from 2011–2021 compared with 63% for IDMs. Yet Europe captures only about 1% of global fabless revenues, with most EU design activity in IDMs and focused on lower-margin mature-node products. **Europe's weak position reflects structural barriers**: extremely high costs for advanced-node tools, IP and engineering talent, limited deep-tech finance, and a fragmented base of small design teams. Addressing these obstacles is essential to give European firms a viable path into higher-value segments of the chip industry.

The Chips Act therefore created the **Design Platform**, a cloud-based EU-wide environment offering shared access to design tools, IP libraries, PDKs and expert support. It aims to expand design capacity, lower entry barriers for start-ups and SMEs, link design to pilot lines and foundries, enable collaboration on new IP and methodologies, and strengthen skills through national competence centres. As the

strategic backbone of the Chips for Europe Initiative, the platform provides a one-stop entry point into the ecosystem, guiding users from design to prototyping and manufacturing, and uniting research, education, and industry. Its ultimate goal is to foster a new generation of European fabless start-ups, a crucial endeavour because these companies capture the highest value in the semiconductor value chain, drive innovation in fast-growing markets, and reduce Europe's dependence on foreign design ecosystems.

Quantum chips

To recognise the **strategic importance of quantum computing**, the Initiative aimed to accelerate development of quantum chips and associated technologies, including those based on semiconductor material or integrated with photonics. Dedicated actions include design libraries for quantum chips, pilot lines for building quantum chips, and facilities for testing and validating quantum chips produced by the pilot lines. The aim is to provide European researchers, start-ups and industry with reliable access to facilities capable of producing and validating the main quantum chip technologies ([17]).

Quantum technologies represent a **frontier technology** domain where semiconductor manufacturing capabilities will determine future competitive positioning. Quantum computing systems fundamentally rely on specialised quantum chips that require advanced semiconductor fabrication, cryogenic electronics, integrated photonics, and novel packaging solutions. The Chips Act's inclusion of quantum chips addresses the strategic imperative to establish European capabilities at the intersection of quantum technologies and semiconductor manufacturing. This early-stage intervention recognises that quantum computing, quantum communication, and quantum sensing applications all depend on semiconductor-based components, making quantum chip development integral to both semiconductor industrial strategy and quantum technology development.

Competence centres

Beyond infrastructure, the Initiative also addressed the Union's skills gap by enabling each Member State to establish **at least one semiconductor competence centre** in their territories. These centres constitute a central pillar of the Chips for Europe Initiative, providing structured access to technical expertise, testing facilities, and advisory services, and enabling companies (particularly SMEs and start-ups) to strengthen their design capabilities, experiment with new technologies, and develop specialised skills.

Acting as **national/regional entry points** to the European semiconductor ecosystem, competence centres facilitate knowledge and technology transfer, support the uptake of innovation, help connect stakeholders with technology infrastructures, and inform about funding opportunities. Competence centres also support access to publicly funded infrastructures, including pilot lines, testing facilities, and other competence centres.

Moreover, competence centres are tasked with supporting **skills development**, including by fostering cooperation with higher education and vocational training providers, and by enhancing the visibility and attractiveness of the semiconductor sector.

([17]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative

Chips Fund

Finally, the Commission established a dedicated semiconductor **investment facility** as part of the Initiative. Referred to collectively as the '**Chips Fund**', it provides both equity and debt financing, including through a blending facility under the InvestEU Fund established by Regulation (EU) 2021/523, in cooperation with the European Investment Bank Group and other implementing partners.

The Chips Fund is intended to complement public investment in research and infrastructure by improving **access to finance for start-ups, SMEs, and scale-ups** across the semiconductor value chain. By facilitating the mobilisation of private capital and offering financing instruments adapted to different stages of company growth, the Fund supports the commercialisation of innovation and the scaling of promising technologies. In doing so, it helps **translate advances made under the Initiative into viable business activity** and contributes to the development of a more dynamic and resilient European semiconductor ecosystem.

2.1.3.2. Pillar II - Security of supply and resilience

Pillar II was conceived as the **'industrial backbone' of the Chips Act**, responding to a structural weakness in Europe's semiconductor policy framework that predated the Regulation. For many years, the cost of advanced semiconductor manufacturing had increased sharply, making new fabrication projects highly capital-intensive and financially risky. In a global context where major competitors were increasingly supporting fabs through large public subsidies, firms lacked comparable instruments to de-risk investment and commit to production capacity in the Union. As a result, Europe's investment in state-of-the-art manufacturing continued to lag behind Asia and the United States, and its share of global semiconductor capital expenditure declined to around 4% and stagnated for over a decade, with only limited authorised State aid ([18]). Pillar II was therefore designed to introduce a **dedicated framework for enabling and attracting manufacturing investment**, by creating legal certainty for public support to First-of-a-kind (FOAK) facilities.

Its objective was not only to **increase manufacturing capacity** but also to restore Europe's credibility as an **investment destination** in a highly competitive global market. To this end, Pillar II established criteria to recognise and support **Integrated Production Facilities (IPF) and Open EU Foundries (OEF)** that are FOAK facilities and that fostered the security of supply and the resilience of the Union's semiconductor ecosystem. These facilities are pioneering and innovative manufacturing plants that do not yet exist in Europe. They may obtain the status of either an IPF – a vertically integrated site engaged in chip design, front-end manufacturing, equipment production, and back-end services – or an OEF, which allocates a defined share of its production capacity to manufacturing chips for external customers. The Regulation designated these facilities as being in the public interest, allowing Member States to apply support measures and provide administrative support in national permit-granting procedures.

The second pillar provides the tools and instruments to address the above-mentioned Strategic Objectives 3) and 4).

([18]) ECA special report 12/2025 – para. 44 - https://www.eca.europa.eu/ECAPublications/SR-2025-12/SR-2025-12_EN.pdf

2.1.3.3. Pillar III - Monitoring and crisis response

Pillar III was introduced to address the absence of any structured EU-level mechanism for **anticipating semiconductor shortages and coordinating responses** to major supply disruptions. Before the Chips Act, monitoring of the sector was fragmented across Member States and institutions, and crisis responses depended largely on national measures taken in isolation. Pillar III therefore created via the European Semiconductor Board a **permanent framework for joint mapping, monitoring and information exchange** between the Commission and Member States.

The architecture was designed not only to improve situational awareness but also to provide a **coordinated toolbox** in the event of crises, including targeted information requests, prioritisation of orders for critical sectors, and joint purchasing. The importance of this pillar has increased in a context of **intensified geopolitical tension**, **reshaped global value chains** and growing recognition of **semiconductors as a strategic asset**. By shifting from reactive crisis management to structured preparedness, Pillar III strengthens the EU's resilience, its capacity to anticipate vulnerabilities and respond collectively.

The third pillar provides the tools and instruments to address the above-mentioned Strategic Objective 5).

2.1.4. Inputs to the Chips Act

The Chips for Europe Initiative was supported by **funding from Horizon Europe and the Digital Europe Programme**, for a maximum indicative amount of EUR 1.725 billion and EUR 1.575 billion respectively, totalling EUR 3.3 billion. Except for the Chips Fund, the implementation of the Chips for Europe Initiative was entrusted to the Chips Joint Undertaking established by Council Regulation (EU) 2023/1782 of 25 July 2023, amending Regulation (EU) 2021/2085.

The implementation of the Chips Act involved **close coordination between the Union, Member States, and the private sector**. The **European Semiconductor Board**, composed of representatives of the Member States and chaired by the Commission, was established to facilitate a smooth, effective and harmonised implementation of the Regulation, cooperation, and the exchange of information. The monitoring and crisis response mechanism was implemented through administrative and coordination structures, primarily the ESB, rather than through dedicated funding programmes.

2.1.5. Expected outputs, results, and impacts

The evaluation of the EU Chips Act examines whether its instruments are appropriate and whether the implementation of activities and **outputs** has led to the expected **results** and **impacts**. Results reflect medium-term changes stemming from the Act's outputs, while impacts represent the longer-term transformations it seeks to achieve. Just over two years after entry into force, early results show initial progress toward the Act's objectives. These are the immediate consequences of the first implementation phases. While outputs and short-term results are largely within the control of implementing authorities, longer-term results and impacts are shaped by external factors such as geopolitical instability, trade tensions, rapid technological change, rising demand, material scarcity, and global competition.

Across its three pillars, the Act has generated several **outputs** and short- and medium-term **results**:

- Pillar I aimed to deliver interconnected results in investment, innovation capacity, skills, collaboration and governance. Increased investment was expected as public funds leveraged private capital. The Act sought to expand the talent pool and address skills gaps through training and education initiatives (while recognising Member State competences). Benefits for industry included improved stakeholder collaboration, better access to funding, and higher rates of technology transfer to accelerate innovation.
- Pillar II delivered outputs through FOAK facility recognition and State aid approvals, leading to a number of supported facilities and contributing to enhanced EU capacity across the value chain via advanced manufacturing capabilities.
- Pillar III established coordination mechanisms for mapping and monitoring the semiconductor ecosystem, including the ESB, emergency toolbox, and SCAN methodology. These were expected to improve global supply chain monitoring, visibility and preparedness, and create synergies with EU, national and regional initiatives, strengthening governance across the semiconductor landscape.

Impacts represent the fundamental long-term changes the Act aims to achieve. They measure progress toward strategic objectives and often materialise only after initial results interact with wider policies and market forces. Causal links are less direct due to external influences. The Act's primary expected **long-term impact** is a strengthened, more resilient Union-level semiconductor ecosystem, with increased domestic production reducing dependence on third countries and enhancing Europe's economic security. A second expected impact is contributing to the EU's target of reaching 20% global semiconductor market share by 2030 under the Digital Decade Policy Programme, solidifying Europe as a major player. Ultimately, the Act aims to foster innovation leadership and sustained growth by building a competitive ecosystem that supports the Digital Decade, the Green Deal, and a more prosperous, technologically secure Europe.

2.2. Points of comparison

The evaluation attempts to **capture progress** in the implementation of the Chips Act and the **changes observed** as a result of its implementation.

Annex II of the Chips Act sets out measurable indicators to monitor the implementation and report on the progress towards the achievement of operational objectives. The performance of the intervention can be measured against the process on these indicators over time, as well as core outputs, combined with a selection of indicators on expected results and impacts – as highlighted in the intervention logic and evaluation matrix (see Annex I – Evaluation matrix).

The main points of comparison are:

- The situation before the intervention (2021);
- The situation during the evaluation of the Chips Act (using monitoring data, evaluation and impact assessment findings, 2025).

Please refer to Annex II – Main points of comparison.

3. HOW HAS THE SITUATION EVOLVED OVER THE EVALUATION PERIOD?

3.1. The implementation of the Chips Act

3.1.1. Pillar I

Pillar I ([19]) (see Section 2.1.3.1) focuses on supporting technological capacity building and innovation in the Union, boosting research and development (R&D), strengthening Europe's research and technology leadership, and accelerating the transition from research to industrial-scale production ('*bridging the gap from lab to fab*').

With the exception of the Chips Fund (which is being implemented by the European Innovation Council and InvestEU), the Initiative is implemented through the **Chips Joint Undertaking (Chips JU)** ([20]), previously known as the Key Digital Technologies Joint Undertaking ([21]). The Union contributes up to EUR 4.175 billion from the Digital Europe Programme (DEP) and the Horizon Europe (HE) programme to the budget of the Chips JU between 2021 and 2027, including EUR 2.875 billion for the Chips for Europe Initiative. Union funding is commensurately matched by Member States and associated countries (participating states). Industry contributes an amount of at least EUR 2.5 billion. On the other hand, the Chips Fund is funded with an amount of EUR 425 million from the Union's budget which is expected to trigger a total amount of around EUR 2.1 billion EU investment and leveraged equity support.

Two years after its entry into force, **more than 85% of the Initiative's budget has already been committed** in order to connect top-tier research with industrial applications ([22]). Because of the complexity of the Initiative's various components, certain activities have progressed faster than others. For example, while competence centres are operational and five pilot lines are starting operations, the design platform is expected to become fully operational in the second half of 2026.

Below, the status of implementation of each operational objective is presented in detail.

Pilot lines

As explained in Section 2.1.3.1, the **pilot lines** are intended to serve as platforms for European research and development with an industrial perspective to bridge the gap between the Union's advanced research and innovation capabilities and their industrial exploitation ([23]).

In the beginning of December 2023, barely two months after the Chips Act's entry into force, the **first four calls for pilot lines** were launched by the Chips JU. While the pilot lines are currently operational to varying extents, more equipment, machinery, and tools are being added to increase the capability and capacity of the pilot lines. Some parts incur delays, typically linked to delays in the procurement of tools and equipment. In any case, the Commission expects full capacity to be achieved by the end of 2026. In July 2024,

([19]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative
([20]) https://www.chips-ju.europa.eu/
([21]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative
([22]) https://digital-strategy.ec.europa.eu/en/news/european-chips-act-update-latest-milestones
([23]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-chips-europe-initiative

the Chips JU launched a **call for a fifth pilot line** on photonics which would see its first operation by the end of 2025 and achieve full capacity also by the end of 2026.

In line with the technology areas laid down in the Chips Act ([24]), the Chips JU launched calls for pilot lines supported with a total of EUR 3.7 billion public funding ([25]) that focus on five key areas (see Section 2.1.3.1):

Pilot line	Name	Coordinator	EU funding (in EUR million)	National funding (in EUR million)
Leading edge nodes	NanoIC	IMEC (BE)	700.0	700.0
FDSOI	FAMES	CEA-Leti (FR)	414.7	414.7
Heterogeneous integration	APECS	Fraunhofer (DE)	366.4	366.4
Wide-bandgap materials	WBG	CNR (IT)	160.2	191.0
Photonics	PIXEurope	ICFO (ES)	189.9	189.9
Total			1,831.2	1,862.1

In addition to these pilot lines, a dedicated **Accelerator for Advanced Strained SOI Substrates (sSOI Accelerator)** was introduced in the Chips JU's 2025 work programme with an EU contribution of EUR 30 million. The topic aims to establish a European supply of strained silicon-on-insulator wafers, enabling 7 nm fully-depleted SOI technology by 2030 ([26]). Selection decisions will be made in Q1 2026.

Moreover, on 15 November 2025, the Chips JU launched a EUR 50 million call on "**Lab to Fab Accelerators**" for advanced packaging and heterogeneous integration and a corresponding EUR 2 million *Coordination and Support Action* to boost cooperation for industrial implementation of advanced packaging of chiplets and heterogeneous integration in Europe. The aim of these two calls is to achieve a **rapid uptake by European industry of the technologies developed under the pilot lines**, in particular technologies related to advanced packaging.

Design platform

Setting up the Design Platform (see Section 2.1.3.1) is particularly complex because it involves a wide range of actors (Platform Coordination Team (PCT), Design Enablement Teams (DETs), cloud providers, Electronic Design Automation (EDA) vendors and IP providers) and follows sequential implementation steps. These run from appointing the PCT and defining specifications to launching subsequent calls and the tender for the central cloud platform, making it slower to establish than other Initiative components. Funded under DEP and HE, the platform is structured through seven interlinked calls.

A PCT is now in place to operate the platform, host the central cloud infrastructure and coordinate user support services. DETs have also been selected to provide tailored, end-to-end support for users throughout the chip development process. A tender is currently open for the central cloud infrastructure, which will host IP, pilot-line Process Design

([24]) Chips Act, Article 5 and Annex I
([25]) https://digital-strategy.ec.europa.eu/en/news/chips-europe-initiative-milestone-event-first-pilot-lines
([26]) https://www.chips-ju.europa.eu/Appendix6_I.pdf

Kits and open-source EDA tools. Another call is open to administer grants for start-ups and SMEs using the platform.

As part of the broader objective to support design, the Design Platform is complemented by other initiatives aiming to cultivate design related competences in Europe. There is support for open-source EDA tools development and for the EuroPractice services that provide over 600 European universities with access to EDA tools for training at nominal costs as well as access to fabrication from leading foundries.

Quantum chips

The Chips for Europe Initiative also focuses on the specific needs of chips exploiting quantum effects, i.e., quantum chips (see Section 2.1.3.1). This is a sector in which the EU remains competitive ([27]). This is confirmed by a recent JRC report that concludes that overall, the EU is well-positioned to play a key role in the development of quantum technologies, with its strong research and innovation ecosystem, and significant investments in the sector ([28]). The aim is to provide European researchers, start-ups, and industry with reliable access to facilities capable of producing and validating the main quantum chip technologies.

In September 2024, the Chips JU launched two calls that led to the establishment of Framework Partnership Agreements launching six pilot lines, **one for each of the leading European technology platforms: superconducting, spin, photonic, diamond, neutral-atom, and trapped-ion chips.** In July 2025, the selected consortia were invited to submit Specific Grant Agreement proposals, each with an indicative EU contribution of EUR 25 million, to be matched by participating states ([29]). These SGAs cover the first three to four years of implementation under each FPA. Their work focuses on setting up stable pilot-scale fabrication processes, integrating testing and experimentation facilities, developing early industrialisation roadmaps, and laying the groundwork for future scaling. These steps mark the initial phase of a broader EUR 200 million EU investment matched by participating states in quantum chip development foreseen under the Chips Act until 2027 ([30]).

([27]) ZVEI, https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20; DigitalEurope, Chips Act 2.0: From emergency response to strategic industry development - DIGITALEUROPE

([28]) https://publications.jrc.ec.europa.eu/repository/handle/JRC141050

([29]) https://www.chips-ju.europa.eu/Appendix6_I.pdf

([30]) https://digital-strategy.ec.europa.eu/en/news/european-chips-act-update-latest-milestones

Pilot line	Name	Coordinator	EU funding (in EUR million)	National funding (in EUR million)
Superconducting	SUPREME	VTT (FI)	25.0	24.2
Spin	SPINS	IMEC (BE)	24.8	23.2
Photonic	P4Q	University of Twente (NL)	24.9	26.6
Diamond	DIREQT	CNR (IT)	25.0	24.5
Neutral-atom	Q-PLANET	PASCAL (FR)	25.0	21.8
Trapped-ion	CHAMP-ION	SAL (AT)	25.0	20.7
Total			149.7	141.1

Competence centres

Competence centres in semiconductors (see Section 2.1.3.1) play an **essential role in the Initiative**. The centres provide access to technical expertise and experimentation in the area of semiconductors, helping companies – SMEs in particular – to approach and improve design capabilities and developing skills.

As of end of 2025, following two Chips JU calls, competence centres have been established in all Member States, as well as in Norway. For these calls, the Union made available for each competence centre up to EUR 1 million per year, per country, for a 4-year period, while participating states made a matching contribution. In addition, a *Coordination and Support Action (CSA)* was launched to set up and coordinate the work of the national competence centres.

Skills

Competence centres have the mandate to support skills development, including networking higher education and vocational training opportunities, and promoting the sector's visibility and attractiveness. The CSA in charge to set up the network of competence centres has launched a **Training and Skills Development** focus group which drives collaboration among the centres to roll out education and upskilling initiatives, to create training concepts, and to provide specific training and access to the design platform and pilot lines.

The Union of Skills calls for a reinforced **Pact for Skills** where Large-Scale Partnerships will support the development of sector-specific solutions; it will tackle the fragmentation of initiatives and improve linkages between them, such as the EU Skills Academies, European Alliance for Apprenticeships, the Centres of Vocational Excellence and European Universities alliances. Improvements will be made to cross-sectoral synergies among Pact members, knowledge and resource sharing along the value chain (e.g. skills intelligence, occupational profiles, curricula, training modules). The existing **microelectronics partnership** is already providing upskilling and reskilling opportunities in the sector. Through its activities, it promotes upskilling and reskilling of 50% of the workforce each year by 2030 across the industry.

Under the **Union of Skills**, the STEM Education Strategic Plan aims to strengthen the talent pipeline in STEM sectors from early education through lifelong learning. The Plan's actions target schools (including through the establishment of STEM Education Centres), higher education institutions (including through the establishment of European

Degrees in Engineering), companies (including through the creation of STEM Skills Foundries) and girls and women (including through the initiative 'Girls Go STEM'). A Commission expert group 'STEAM Executive Panel' will provide advice and recommendations to the Commission on how to strengthen academia-business collaboration.

Another skills related action is the **European Chips Skills Academy** (ECSA), a four-year European Blueprint project funded under Erasmus+ and kicked off in October 2023. It brings together a wide range of key players in the microelectronics ecosystem and opens new opportunities for collaboration between industrial leaders and educational institutions at all levels (secondary school, VET providers, and higher education). It has been focusing on mapping the skills needs and demand by industry, developing innovative strategic approaches and collaboration between education and businesses, and bridging its gap with VET and higher education ([31]).

Moreover, the Chips JU 2026 work programme contains three topics on talent development, worth EUR 45 million, which will support and complement initiatives by the competence centres on higher education, vocational training, and hands-on activities for students and workers. **These 2026 topics and the Competence centres' activities support the wider Commission's strategy on skills** and build on some recent initiatives launched by the Commission, such as the calls of the 2022, 2023 and 2024 DEP Work Programmes (EUR ~28 million), ongoing projects under Erasmus+ such as the above-mentioned European Chips Skills Academy (EUR ~4 million) and the European Chips Diversity Alliance (EUR ~1.5 million) ([32]), the Industrial Alliance on Processors and Semiconductor Technologies ([33]) and notably its working group on skills ([34]), and the Chips Academy call foreseen by the current DEP Work Programme in 2027 (EUR ~10 million).

Chips Fund

The Chips Fund aims to improve access to capital for start-ups, scale-ups, SMEs, and other companies in the semiconductor value chain. It is currently implemented through two thematic investment facilities:

- European Innovation Council's Accelerator programme, with Horizon Europe funding in blended grant and equity for high-risk, deep-tech startups.
- InvestEU Fund, managed by the European Investment Fund (EIF), with a guarantee from DEP, for intermediated equity investments ranging from seed to growth stage.

Under the Chips Fund, the **European Innovation Council (EIC)** has launched a dedicated **Accelerator Challenge on Semiconductor and Quantum Technologies** in its 2023 and 2024 work programmes, through which 24 highly innovative startups were selected and awarded a total of EUR 62 million in grants and EUR 238 million in

([31]) https://chipsacademy.eu/
([32]) https://diversityinchips.eu/
([33]) https://single-market-economy.ec.europa.eu/industry/industrial-alliances/industrial-alliance-processors-and-semiconductor-technologies_en
([34]) https://allpros.eu/thematic-working-groups/working-group-skills

recommended equity investment from the EIB, and mobilising further private capital. **The EUR 300 million available budget was fully deployed in just two years**.

Beyond this thematic window, semiconductor, photonics and quantum chip companies continue to be eligible under the **open EIC Accelerator call**, where they compete with applicants from all fields; it is estimated that between 2020 and 2025 an additional EUR 500 million in grants and equity were allocated to beneficiaries from these domains through the open calls.

Complementing this, from 2025 the **Strategic Technologies for Europe Platform (STEP) programme** has been implemented with a call targeting deep-tech scale-ups in digital, deep tech, clean tech, and biotech, with a budget of EUR 300 million per year. Semiconductor and quantum scale-ups are explicitly included, and eight such companies have already been selected for a total recommended equity investment of EUR 180 million, that would address the chronic lack of scale-up capital for deep-tech semiconductor firms in Europe.

On the **InvestEU** leg of the Chips Fund, the Commission provides a EUR 125 million guarantee, matched by EIF resources and implemented by the EIF as an intermediated fund through a thematic investment facility on "Semiconductor chips and technologies". The final selection of portfolio companies is carried out by financial partners (venture capital funds) selected by the EIF. To date, four financial partners have been selected and EUR 68 million in funds have been signed or approved with them, with two additional partners currently in the due diligence pipeline, resulting so far in 31 companies from early to growth stage having received EUR 116 million equity investment.

European Chips Infrastructure Consortium – ECIC

For the purpose of implementing actions funded under the Chips for Europe Initiative, Article 7 of the Chips Act introduces the possibility for consortia to establish a legal entity in the form of a **European Chips Infrastructure Consortium** (ECIC). The main benefit of an ECIC is the fact that it has legal personality (and hence, legal capacity in all Member States). This means, for instance, that compared to some other instruments, its duration extends beyond the lifetime of a given Multiannual Financial Framework, granting an ECIC certain stability. Moreover, an ECIC whose membership would not include private entities would be recognised as an international body, which could have certain VAT advantages. While ECICs could implement any action under the Initiative, they were mainly meant to implement pilot lines or the design platform.

Since the Chips Act's entry into force, **the Commission did not receive any application to set up an ECIC**. The initiative to set up an ECIC belongs to the coordinator of a potential consortium. For instance, the consortia that are implementing the five pilot lines and the design platform opted for a traditional project consortium structure.

3.1.2. Pillar II

Pillar II is aimed at attracting significant public and private investments in innovative FOAK production facilities ([35]) that may be granted the **status of IPF or OEF** (see Section 2.1.3.2). Benefits of such status include administrative support in national

([35]) Chips Act, articles 13-18.

permit-granting procedures, and prioritised access to pilot lines. At the same time, where a semiconductor crisis stage is activated by the Council (Article 23 Chips Act), the Commission is enabled to require IPF and OEF facilities to accept and prioritise an order of crisis relevant products ('priority-rated order'). **Nevertheless, both the activation of the crisis stage and the application of priority-rated orders have not been used so far**. They are 'last resort' measures subject to very specific criteria and conditions that ensure that they are necessary and proportional.

FOAK facilities

Although applying for the status of IPF or OEF is not mandatory and requires a separate procedure from the State aid assessment, these two procedures and the respective assessments are typically conducted in parallel, where possible ([36])([37]). The application process and eligibility criteria for applications are outlined in the guidance prepared by the Commission ([38]).

While **several projects are still under development**, the Commission has already approved **eleven State aid decisions on FOAK semiconductor facilities** that represent a total public and private investment of over EUR 32 billion ([39]). Out of these cases, the Commission has formally granted the status of IPF and OEF to four semiconductor projects ([40]) in October 2025, while more are in the pipeline. The projects that received the status include OS4EU (ams OSRAM, Austria), ESMC (European Semiconductor Manufacturing Company, Germany), MEGAFAB-DD (Infineon Technologies Dresden, Germany), and Catania Campus (STMicroelectronics, Italy) ([41]).

Company	Location	Investment (in EUR billion)	Technology
STMicroelectronics	Catania (IT)	0.73	SiC wafer
STMicro & GlobalFoundries	Crolles (FR)	7.5	300-mm FD-SOI
STMicroelectronics	Catania (IT)	5	SiC devices
ESMC	Dresden (DE)	>10	CMOS, FinFET
Silicon Box	Novara (IT)	3.2	Advanced packaging
Infineon	Dresden (DE)	3.54	Discrete, analog/mixed signals
ams OSRAM	Premstätten (AT)	0.567	CMOS
Ephos	Milan (IT)	n.d.	glass-based photonic chips
onsemi	Rožnov (CZ)	1.64	SiC devices
GlobalFoundries	Dresden (DE)	n.d.	300-mm FD-SOI and BCD
X-Fab	Erfurt (DE)	n.d.	Advanced packaging

([36]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-security-supply-and-resilience
([37]) FOAK compliance and some obligations associated with IPF/OEF status are taken into account in the State aid assessment (cfr. Chips Act Communication, https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=celex:52022DC0045)
([38]) https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=OJ:C_202404911
([39]) https://digital-strategy.ec.europa.eu/en/policies/european-chips-act
([40]) https://digital-strategy.ec.europa.eu/en/news/milestone-strengthening-europes-semiconductor-manufacturing-capacity-under-chips-act-reached
([41]) https://digital-strategy.ec.europa.eu/en/library/commission-decisions-strengthening-europes-semiconductor-manufacturing-capacity-under-chips-act

Total	>32

n.d. = not disclosed (yet)

These investments under Pillar II are complemented by an **Important Project of Common European Interest ('IPCEI')** on microelectronics and communication technologies, which supports research and development up to first industrial deployment across the value chain with over **EUR 20 billion** total public and private investment ([42]). Moreover, a number of additional projects have been announced, are in preparation or in the decision process, with estimated value around EUR 25 billion. Taking all together, including support for the IPCEI on Microelectronics and Communication Technologies, so far, **the Chips Act has already catalysed more than EUR 80 billion in announced or planned investments in chip manufacturing capacity as well as related research and innovation investments**, thereby contributing to increasing the EU's market share globally.

Label of design centres of excellence

According to Article 17 of the Chips Act, the Commission may award a label of "design centre of excellence" to design centres established in the Union that significantly enhance the Union's capabilities in innovative chip design through their service offerings or through the development, promotion, and strengthening of design skills and capabilities. The procedure for applications and the requirements and conditions for the granting, monitoring, and withdrawal of the label should be set out by the Commission by means of delegated acts ([43]). However, for the reasons explained under Section 4, at the point of this evaluation, the Commission did not adopt delegated acts on design centres of excellence.

3.1.3. Pillar III

Pillar III is dedicated to **enhancing cooperation between EU Member States and the European Commission** to anticipate future chips crises, and to address them through close coordination. To this end, the ESB is tasked with monitoring and crisis response activities, and with advising the Commission across all three pillars. The coordination mechanism consists of three components:

- **Monitoring**: strategic mapping; early-warning indicators; identification of key market actors; risk mitigation;
- **Crisis response**: alerts and preventive actions; activation of the crisis stage; emergency toolbox (including information gathering, priority-rated orders, and common purchasing);
- **Governance**: European Semiconductor Board.

The preparatory work started in 2022 with the Commission's Recommendation on a common Union toolbox to address semiconductor shortages and an EU mechanism for monitoring the semiconductor ecosystem ([44]). A **European Semiconductor Expert Group** was established through which Member States implemented the

([42]) https://ec.europa.eu/commission/presscorner/detail/en/ip_23_3087
([43]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-security-supply-and-resilience
([44]) Commission Recommendation (EU) 2022/210 of 8 February 2022 on a common Union toolbox to address semiconductor shortages and an EU mechanism for monitoring the semiconductor ecosystem

Recommendation. The formal work on the monitoring mechanism began once the Chips Act regulation had entered into force in September 2023, and the ESB was formally set up. The Commission signed a service contract in September 2025 ([45]) to provide analytical, methodological, and administrative support to the Commission and the ESB in the implementation of Pillar III.

Monitoring

The Commission, in consultation with the ESB, **monitors the semiconductor value chain to identify possible disruptions**. This monitoring foresees a strategic mapping of the sector, including key products and critical infrastructures, main user industries, and key segments of the supply chains and dependencies; monitoring of early warning indicators; Member States' reporting on market trends; and best practices for preventive risk mitigation and increased transparency.

Regarding the status of implementation, the **key mapping and data collection** took place and the **analysis of supply chains** has been developed. Several key reports have been published to address these issues, including the JRC report "Semiconductors in the EU" ([46]), report "The EC consultation on the semiconductors' value chain" ([47]), report "Economic analysis of the EU and international semiconductor ecosystem" ([48]), and JRC report "EU's strengths and weaknesses in the global semiconductor sector" ([49]). Furthermore, the **SCAN monitoring system** was established, alongside the detailed monitoring methodology ([50]). The complete methodological toolbox proposed to monitor the semiconductor supply chain, including the SCAN methodology, was outlined in the following JRC reports: "Applying the SCAN methodology to the Semiconductor Supply Chain" ([51]) and "A methodological toolbox to monitor the semiconductors' supply-chain" ([52]).

Moreover, in 2023, a **semiconductor alert system** was set up to allow stakeholders to report semiconductor supply chain disruptions. It helps the Commission to gather information needed to establish a precise assessment of risks and to quickly react to any potential crisis situation via the ESB ([53]).

Economic Security

([45]) https://ted.europa.eu/en/notice/-/detail/627092-2025
([46]) https://publications.jrc.ec.europa.eu/repository/handle/JRC133850
([47]) https://publications.jrc.ec.europa.eu/repository/handle/JRC133892
([48]) https://icos-semiconductors.eu/uncategorized/economic-analysis-of-the-eu-and-international-semiconductor-ecosystem/
([49]) https://publications.jrc.ec.europa.eu/repository/handle/JRC141323
([50]) The SCAN monitoring system is an internal system used by the Commission, which mainly tracks the product dependencies at EU and Member State level leveraging customs data. The methodological toolbox will be implemented via the service contract signed in September 2025 (by among others gathering supply chain data to frequently generate and monitor the proposed indicators).
([51]) https://publications.jrc.ec.europa.eu/repository/handle/JRC133736
([52]) https://publications.jrc.ec.europa.eu/repository/handle/JRC138921
([53]) https://digital-strategy.ec.europa.eu/en/news/european-chips-act-commission-launches-pilot-system-monitor-semiconductor-supply-chain

The **EU Economic Security Strategy** ([54]) is a separate policy from the Chips Act, and therefore not in the scope of the evaluation. However, strong links organically emerged between the Strategy and the Chips Act, in particular with Pillar III. The Strategy mandated **joint Risk Assessments** with Member States on Advanced Semiconductor technologies ([55]). A subgroup of the ESB was created to collect data, and to validate the draft reports before adoption by the plenary. A first report covered the **risks for the security of supply of advanced semiconductors linked to tensions in the Indo-Pacific**, and showed that a severe shortage or denial to access of semiconductors would have a significant impact for EU companies in essential sectors for the European economy, including the automotive, space and defence, and telecommunication sectors. A second report covered the risks of **semiconductor-manufacturing equipment technology leakage to third countries**. The main risks identified are a loss of market share and competitive edge, and erosion of the EU's technology leadership and indispensability.

Crisis response

Article 24 of the Chips Act establishes a **crisis response mechanism** (i.e., "emergency toolbox") that the Commission may use when serious semiconductor supply-chain disruptions endanger the supply, repair or maintenance of essential products for critical sectors. The Commission may consult the ESB on preventive actions such as joint procurement and policy coordination within the EU and with third countries. If it considers a **crisis stage** necessary and proportionate, it may propose its activation to the Council. Once activated, the Commission increases coordination with the ESB and may apply one or more emergency tools. Annex IV of the Chips Act lists the critical sectors concerned, including energy, transport, banking and financial infrastructure, health, water and wastewater, digital infrastructure, public administration, space, food production and distribution, defence and security ([56]).

At the point of this evaluation, a crisis has not been activated since the entry into force of the Chips Act. There have been examples of supply chain disruptions that however did not qualify as a crisis according to Article 23 of the Chips Act, for instance because they involved sectors not included in Annex IV. Moreover, in order to assess whether or not critical sectors are threatened, a swift review of available evidence is necessary, as the Nexperia case (see Section 4.1.1.3) made evident. In this case, the Commission created the **Task Force on Situational Analysis**, a subgroup of the ESB composed of a small number of experts volunteered by 8 Member States ([57]). It assists the Commission in the collection and analysis of evidence regarding rapidly developing situations or imminent risks to economic security in the field of semiconductors, when coordinating 27 Members would be too slow. The Taskforce reports its finding to the ESB.

([54]) https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=celex:52023JC0020
([55]) https://digital-strategy.ec.europa.eu/en/news/commission-recommends-carrying-out-risk-assessments-four-critical-technology-areas-advanced
([56]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-monitoring-and-crisis-response. See also Annex IV of the Chips Act.
([57]) https://ec.europa.eu/transparency/expert-groups-register/screen/expert-groups/consult?lang=en&fromMainGroup=true&groupID=105752

In case a crisis is activated, **Pillar III's toolbox includes three measures**: information gathering (Article 25), priority-rated orders (Article 26) and common purchasing (Article 27).

Under the first measure (**information gathering**), the Commission may request undertakings operating along the semiconductor supply chain to provide information about their production capabilities and capacities, as well as current primary disruptions. **This measure is ready for deployment**.

Under the second measure (**priority-rated orders – PROs**), a semiconductor company may be requested to accept and preferentially perform an order of crisis-relevant products for an individual beneficiary of a critical sector. **This measure is not yet ready for deployment**, because, on the one hand, facilities that may be subject to PROs will only be operational as of 2028. On the other hand, at the moment of finalising this evaluation report the Commission has not yet adopted the implementing act laying down the practical and operational arrangements for the functioning of PROs.

The third measure (**common purchasing**) allows the Commission, upon the request of two or more Member States, to act as a central purchasing body on behalf of all Member States willing to participate for their public procurement of crisis-relevant products. While this measure is **legally ready for deployment**, preparatory work is still ongoing internally in order for the Commission to be ready to take up the **role of central purchasing body**. This is due to the fact that common purchasing qualifies as public procurement from the Union and would therefore require preparation and coordination between different services in charge of technical, legal and budgetary aspects. A standard operating procedure is in preparation to define an appropriate workflow.

Governance – European Semiconductor Board

The governance mechanism of the Chips Act is ensured by the **ESB** ([58]), which includes representatives of the Member States and is chaired by the Commission. **The ESB has been actively steering progress since November 2023**, coordinating national efforts and monitoring supply chain resilience. The ESB provides the Commission with advice, assistance, and recommendations across the three Pillars of action. It advises on the Chips for Europe Initiative to the PAB of the Chips JU (Pillar I); it is consulted for the decisions of the Commission to grant the status of IPF and OEF (Pillar II); and it is responsible for the monitoring and crisis response activities (Pillar III) ([59]).

The ESB is fully operational. Since its inception it has held ten plenary meetings (two online and two physical meetings per year) advising the Commission on all Pillars; four meetings of its three subgroups ([60]); and contributed to a written consultation and two risk assessments in the context of the Economic Security Strategy. The ESB also took part in a **simulation exercise on the preparedness for semiconductor supply chain**

([58]) https://ec.europa.eu/transparency/expert-groups-register/screen/expert-groups/consult?lang=en&groupID=3932
([59]) https://digital-strategy.ec.europa.eu/en/factpages/european-chips-act-monitoring-and-crisis-response
([60]) Working Group on Semiconductor Economic Security; Working Group on Chips Act review; and Task Force on Situational Analysis.

disruptions, together with the Council Working Party on Competitiveness and Growth (Industry) ([61]), supported by the ChipDiplo consortium ([62]).

The European Commission organised a **tabletop exercise on semiconductor supply chain disruptions** in Brussels on 24 November 2025, in order to improve Europe's preparedness to respond to a crisis under the EU Chips Act.

The ChipDiplo consortium, co-funded by the EU, facilitated the activity by developing a fictional but plausible scenario affecting global semiconductor manufacturing hubs, leading to disruptions in the supply chain. The exercise involved participants from all 27 Member States, sitting both in the European Semiconductor Board and in the Council Working Party on Competitiveness and Growth (Industry).

Players analysed the effects of a chips shortage on the European industry and in particular on critical sectors of the society and the economy such as energy, transport, health, digital infrastructure, space, security and defence – as defined in the Chips Act. Each Member State was briefed with country-specific information compiled by the Joint Research Centre and produced in the context of the supply chain mapping activities of the Chips Act. Together, participants explored options to mitigate the impact of the crisis, including mechanisms from the Chips Act's crisis toolbox.

The exercise clearly showed the importance for the EU to increase its preparedness and to invest to reduce its dependencies on third countries. It also showed that decision-makers need a mandate to collect precise and reliable data to properly assess supply chain disruptions, even in order to prevent a crisis from materialising.

3.2. Unexpected or unintended changes

Since the Chips Act was proposed in February 2022, an accelerated shift from multi-polarisation to disentanglement in global markets has taken place. The resulting **weaponisation of economic interdependencies** reveals vulnerabilities within European semiconductor supply chains, posing serious risks to European economic security and sovereignty.

Two weeks after the Chips Act was proposed, the **Russian full-scale invasion of Ukraine** on 24 February 2022 caused a tectonic shift in European politics. The war drove up energy prices in Europe which impacted the competitiveness of energy-intensive industries in Europe and harmed European competitiveness. At the same time, Ukraine's response fuelled innovation in the defence sector which showcased a need for trustworthy European semiconductors.

Shortly thereafter, **OpenAI launched ChatGPT**, a generative artificial intelligence chatbot with 800 million weekly active users. The launch became an inflection point for investments in the entire artificial intelligence stack. Software and hardware companies received unprecedented private investments and state subsidies in order for them to finance data centres and compete for talent. These investments spilled over into the semiconductor market sending companies' market capitalisations to unprecedented heights with Nvidia reaching $5 trillion in October 2025. Additionally, state

([61]) https://digital-strategy.ec.europa.eu/en/news/commission-and-member-states-rehearse-coordinated-response-semiconductor-supply-chain-shortages

([62]) https://digital-strategy.ec.europa.eu/en/news/chipdiplo-consortium-selected-support-international-diplomacy-semiconductors

interventions risk leading to distortions of the market level-playing field and result in overcapacities. This further increases the pressure on European competitiveness and threatens the established multipolar trade regime.

Simultaneously, a **race between the United States and China** to reach leadership in emerging technologies ensued. This intensified existing trade tensions and resulted in a tit-for-tat of tariffs, export controls and licence requirements. Especially, tensions around rare earth elements, for which China holds a monopoly, and semiconductor intellectual property introduced uncertainty to the European market and highlighted a need for increased economic security and sovereignty.

As a result of the outlined dynamics, countries started prioritising the **reshoring of production capabilities** which creates pressure on companies to take investment decisions that mitigate political risks. While this leaves Europe vulnerable to supply chain disruptions, it also shows the need for stable investment conditions. Europe can provide a reliable framework for investments, which is part of the reasons why Intel initially agreed to invest into manufacturing in Magdeburg, Germany (see case study in Section 4.1.1.2). However, in September 2024, Intel postponed and then later withdrew its plans, highlighting once again Europe's vulnerability.

In summary, since the Chips Act was proposed in 2022, **the world has shifted dramatically**. Initially, the semiconductor industry was marked by a severe shortage, impacting various sectors and highlighting the need for increased manufacturing capacity. However, as new facilities began to take shape, particularly in Asia and the United States, the industry saw an expansion in supply capabilities. At the same time, demand for semiconductors continues to grow, propelled by advancements in technology (especially AI) and the proliferation of digital devices. These shifts have created a more competitive landscape, emphasizing the urgency for the EU to bolster its domestic semiconductor manufacturing capabilities to remain competitive.

4. EVALUATION FINDINGS

4.1. To what extent was the intervention successful and why?

This section assesses the effectiveness, efficiency, and coherence of the Chips Act in line with the methodology foreseen under the Better Regulation Guidelines ([63]).

4.1.1. Effectiveness

The effectiveness assessment evaluates how far the Chips Act has advanced competitiveness, innovation capacity, and resilience in the EU semiconductor ecosystem, and whether its expected causal chain has operated as intended. As outlined in Section 3, evidence shows **the Act has delivered many foundational outputs**, including over EUR 80 billion in public and private investments mobilised under Pillar II and the establishment of a Member State–Commission coordination mechanism under Pillar III via the ESB. These developments indicate that the organisational infrastructure needed to support Europe's semiconductor ambitions is largely in place.

However, **translating these outputs into results and impacts will take more time**. The Act entered into force only in September 2023, and long development timelines for pilot lines, the design platform, and new fabs mean many capabilities remain early-stage. Structural barriers (such as skills shortages, lab-to-fab transition challenges, and limited demand-side mechanisms) also hinder uptake. Consequently, although the Chips Act has laid essential groundwork and mobilised the ecosystem ([64]), progress towards its intended impacts (reduced dependencies and greater technological sovereignty) is still ongoing. OPC position papers validate these foundational achievements, with stakeholders consistently identifying Pillar I activities (pilot lines, competence centres, and start-up support) as having strengthened Europe's innovation infrastructure and supported technological capacity building, citing concrete examples including support for start-ups and local benefits such as job creation ([65]).

4.1.1.1. Pillar I

The effectiveness assessment of Pillar I examines progress in strengthening the EU's semiconductor research, design, and innovation base. The Initiative introduced new EU-level instruments and structures; **without the Chips Act, support would likely have remained limited to the former KDT JU with fewer strategic priorities**. Mobilising vast national and EU resources has enabled pilot lines, competence centres across all Member States, and shared design and technology infrastructures together forming a long-term framework for advanced capabilities, including design and quantum technologies.

Although most impacts will materialise later, **these foundations significantly expand the EU's capacity to support semiconductor innovation**. OPC results show that 89%

([63]) European Commission – Better Regulation Guidelines and Toolbox (https://commission.europa.eu/law/law-making-process/better-regulation/better-regulation-guidelines-and-toolbox_en).

([64]) ZVEI, https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20

([65]) Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders provided positive assessments of Pillar I's contribution to innovation infrastructure. See also the Synopsis Report.

of respondents reported that the Initiative partially or fully meets its research and innovation objectives ([66]). However, translating outputs into industrial results remains at an early stage: pilot lines are not yet fully operational, competence centres launched only in 2025, quantum pilot lines are being established, and the design platform will be operational in mid-2026. Thus, while foundational assets are in place, further completion, strengthening, and industrialisation are essential to achieve long-term competitiveness and reduced strategic dependencies.

Pilot lines

The five technology-specific pilot lines (see Section 2.1.3.1) under Pillar I have made **substantial progress toward building up technological capacities and advanced technology infrastructures**. The five pilot lines represent some of the most innovative technology infrastructures in the world, securing EUR 3.7 billion in total investment, comprising EUR 1.83 billion EU contribution matched by EUR 1.86 billion national co-funding (see Section 3.1.1).

From an institutional perspective, the pilot lines constitute a significant element within the evolving framework of European innovation governance. The joint co-ownership structures established between the Chips JU and participating Member States create **clear accountability mechanisms** that safeguard public investments whilst enabling collaborative research and innovation. National funding mobilisation achieved approximately 1:1 matching ratios with EU contributions (workshop 14).

Assessing whether pilot lines will effectively bridge the **research-to-industry (lab-to-fab) gap** is premature at this stage of implementation. Pilot lines are projected to reach full operational capacity by end-2026. This is a reasonable timeline given the technical complexity of procuring and installing advanced semiconductor manufacturing equipment. Yet, technology transfer is already underway in specific segments of the value chain. Equipment manufacturers and material suppliers are actively using pilot lines to validate and refine their technologies, creating early spillover effects even before full industrial-scale technology transfer to manufacturing facilities materialises. Workshop consultations emphasise that as pilot lines approach full operational status, priorities should focus on industrialisation of existing facilities to maximise industrial impact (workshop 14). OPC responses suggest that further industrialisation of pilot lines could be supported through State-aid framework reform (GBER revision) and sustained funding support, while end users highlighted the importance of market-driven orientation from the outset ([67]).

Despite the early stage of implementation, OPC results show that 59% of respondents indicated that **the five selected pilot lines partially or fully support the transition from lab to fab** ([68]). Notably, research and technology organisations – who are the

([66]) Open Public Consultation survey (N=97), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (89 out of 97 responses: 76% partial + 13% fully). Question: To what extent does pillar 1 ‘Chips for Europe Initiative’ of the Chips Act deliver on its objectives?

([67]) Open-ended responses to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders provided qualitative suggestions for pilot line industrialisation through State aid framework reforms.

([68]) Open Public Consultation survey (N=96), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (56 out of 96 responses: 45% partial +

stakeholders closest to pilot line operations – expressed the strongest confidence, with 77% indicating partial or full effectiveness in bridging the lab-to-fab gap ([69]). This positive assessment from those directly engaged with the infrastructures suggests that pilot lines are on track to deliver their intended bridging function.

The implementation of the pilot lines has increased businesses' interest in R&D projects and, most importantly, encouraged **cross-segment collaboration between RTOs and industrial actors** ([70]). Their effectiveness is visible globally, as Europe's pilot line approach remains unique compared to R&D programs in the U.S., China, Taiwan, South Korea, and Japan. To maintain this competitive advantage, SEMI Europe recommends to reinforce the pilot line 'ecosystem' by improving synergies between RTOs and industry and ensuring faster approval procedures that support effective industrial uptake ([71]).

In a nutshell, **pilot lines appear to be well suited** as advanced technology infrastructures enabling technology development and verification. Definitive effectiveness assessment must await full operational deployment and sufficient time for measuring industrial technology transfer. Stronger emphasis on industrialisation and clearer State aid guidance would enhance the pilot lines' capacity to achieve their bridging objective.

Design Platform

As the platform is still under development, it is **too early to judge its effectiveness**. However, the intervention is well aligned with the underlying problem, and early implementation steps indicate progress towards tackling the structural barriers that have kept Europe stagnant in the fabless market. The platform has delivered on its set-up and structuring, moving from concept to implementation with the selection, under the Chips JU, of a consortium of 12 leading European research players to act as the Platform Coordination Team, and of 9 DETs that will offer application engineering support services to startups.

The platform is explicitly positioned as the **entry point to advanced European design capabilities** and is complemented by a substantial acceleration and incubation programme for fabless IC, photonic, and quantum start-ups and SMEs, with around EUR 220 million of Chips JU funding, to be matched by participating states, and distributed to selected beneficiaries using the infrastructure.

However, as explained in Sections 2.1.3.1 and 3.1.1, the setting up of this platform is particularly complex and involves many different sequential steps. Therefore, user onboarding will only start in the second half of 2026. Consequently, effectiveness can only be assessed in terms of the above explained readiness and alignment (governance, scope, funding, timelines), while concrete impact on user uptake, number of designs

---

14% fully). Question: To what extent do the five selected pilot lines support the transition from "Lab to fab"?

([69]) Open Public Consultation survey (N=17), data reflecting the percentage of research and technology organisation respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (13 out of 17 responses: 53% partial + 24% fully). Question: To what extent do the five selected pilot lines support the transition from "Lab to fab"?

([70]) Aeneas, EPoSS, Inside, document submitted under the Open Public Consultation, not public.

([71]) SEMI Europe, https://www.semi.org/en/semi-press-release/semi-europe-publishes-30-recommendations-for-a-forward-looking-european-chips-act

brought to tape-out, and strengthening of Europe's design ecosystem will need to be measured at a later stage.

Quantum chips

The Initiative's objective on quantum chips **contributes to establishing European capacity in an emerging technology domain** where early strategic positioning can shape future competitive advantage. Six consortia were selected for pilot lines covering distinct quantum technology platforms (see Section 3.1.1). This multi-pathway approach addresses technological uncertainty in what could be the future winning quantum technology platform by maintaining openness across development pathways rather than prematurely selecting a single or few quantum technology platform directions.

The programme is designed as a long-term foundational research investment. The programme represents effective integration of quantum objectives into the Chips Act framework. The established architecture provides mechanisms for coordinated European quantum chip development. However, the **pathway from research to industrial deployment** presents challenges characteristic of frontier technology development. Effectiveness in achieving industrial translation will depend substantially on factors beyond the programme's direct control, including the emergence of practical applications and evolution of quantum computing markets. The assessment of effectiveness should be calibrated to realistic timescales, recognising that quantum chips represent a strategic capability-building exercise rather than an intervention expected to deliver short-term competitiveness impact.

Competence centres

Competence centres **enable national/regional SMEs and other companies to access semiconductor expertise and equipment** they cannot independently afford, thereby extending benefits beyond traditional players (Workshop 3, 4). They have been launched in 2025 in all EU Member States and Norway to broaden access to semiconductor expertise, technology infrastructures, and training. Given their recent launch, competence centres need to work on their visibility to attract stakeholders, in particular, SMEs (Workshops 5, 12; Interviews 3, 8).

Some stakeholders across design, manufacturing, packaging, automotive and telecoms noted that expected **benefits from competence centre activities are real but may not scale to match rapidly growing needs** for applied engineering and packaging expertise (Workshops 5, 8, 10; Interviews 7, 11). Technological trends such as AI accelerators, chiplet architectures, and power semiconductors were increasingly shaping industrial priorities. To achieve intended objectives, competence centres must scale their activities, expand applied training, improve communication, and effectively connect SMEs to pilot lines and the European design platform in the coming years.

Overall, the competence centres represent an **essential framework for supporting SMEs, start-ups and research actors**, but their recent launch means that time to reach local industry and, in particular, SMEs and startups was short.

When it comes to **skills**, so far competence centres have not yet started developing education and training initiatives, since such activities require proper investigation and planning prior to actual implementation. Thus, from an effectiveness perspective, **the national competence centres did not yet contribute to enlarge and qualify the talent pool Europe needs** to strengthen its ecosystem and support the Chips Act's objectives.

Only preparatory work such as the Training and Skills Development focus group set up by the Support Action coordinating the competence centres has been undertaken. Conversely, once the network of the competence centres will become fully operational, it will benefit from, build on, and complement the wide range of different initiatives already launched by various DGs of the Commission, as listed in Section 3.1.1.

Chips Fund

The Chips Fund has proven to be **highly effective in supporting innovative semiconductor and quantum startups and scale-ups**, attracting private capital, and addressing key financing gaps along the innovation and growth chain (see Section 3.1.1). The EIC Accelerator thematic Challenge saw its entire EUR 300 million budget fully utilized in less than two years. This highlights strong market demand and the Fund's capability to identify and support high-potential companies in these sectors. However, it also highlights that **the budget allocated to the Chips Fund was insufficient considering the demand**. Additionally, semiconductor, photonics, and quantum companies could access the EIC Accelerator open calls, which ensured that also outstanding projects outside the above thematic areas could be funded, with an estimated EUR 500 million in additional grants and equity from 2020 to 2025. Again, strong demand shows that allocated budgets were insufficient.

Similarly, as explained in Section 3.1.1, the **STEP programme has effectively contributed to tackle the structural lack of later-stage risk capital** and supported companies entering capital-intensive expansion. Likewise, within the InvestEU framework, the EIF has through its financial partners extended support to 31 companies strengthening the transition from seed to growth and complementing EIC tools.

While it is premature to assess long-term effects such as market share, industrial capacity, or strategic autonomy, the complete utilization of budgets, robust project pipelines, and coverage of various company lifecycle stages indicate that the initiative is **on track to achieve its goals**. However, rapid budget depletion signifies **insufficient funding**, given the extensive demand in the semiconductor sector ([72]), including photonics and the burgeoning quantum chip segment. Moving forward, to ensure the effectiveness of the Chips Fund, adequate and consistent funding for scaling fabless semiconductor companies centred on leading-edge chip designs will be crucial.

ECIC – European Chips Infrastructure Consortium

As explained in Section 3, potential consortia implementing actions under the Initiative were given the option to establish an ECIC, a legal instrument modelled closely on the EDICs (European Digital Infrastructure Consortia) created under the Digital Decade Policy Programme ([73]). ECICs were included in the Chips Act proposal to enhance the effectiveness of cross-border cooperation by offering a streamlined, EU-recognised governance framework. However, the use of EDICs could not be guaranteed at the time because the DDPP had not been decided at the moment the Chips Act was proposed.

([72]) Open Public Consultation survey (N=96), 28 respondents out of 96 (29%) indicated that despite not having previously applied to the Chips Fund, they will do so in the future.

([73]) https://eur-lex.europa.eu/eli/dec/2022/2481/oj/eng

The accelerated implementation timeline (pilot line calls launched three months after the Act's entry into force) likely limited the feasibility of applying for ECIC status, as consortia focused on preparing technical proposals and relied on familiar legal structures. Although ECIC recognition could have been sought after selection, no applications were submitted, suggesting that expected benefits did not justify the administrative effort. Overall, the ECIC instrument broadens available options and could, in theory, support cross-border project implementation, but its non-use so far shows it has not enhanced the Initiative's effectiveness, though it may still be useful for future large-scale projects.

4.1.1.2. Pillar II

FOAK facilities

Pillar II has been highly effective in triggering a **sharp rise in announced manufacturing investments** from a previously weak baseline, though its impact on EU market share, strategic oversight, and crisis readiness remains in progress. National authorities' targeted survey responses strongly validate the need for EU-level coordination in this area, with 87.5% (21 of 24) agreeing or strongly agreeing that EU-level coordination is necessary for achieving semiconductor sovereignty in investment and manufacturing capacity ([74]). Before the Chips Act's strategy, investment aid for semiconductor fabs was largely impossible outside assisted regions, and EU support focused mainly on R&D rather than large-scale production. As the cost of advanced fabs rose sharply over the past two decades, companies increasingly sought public support to de-risk major capital exposure (support that was readily provided elsewhere). Consequently, Europe's **investments lagged far behind** Asia and the U.S., leading to a prolonged erosion of competitiveness; EU semiconductor **capital expenditure** fell to **about 4%** of the global total and stagnated for over a decade. Only a small number of projects received EU-approved State aid. As indicated in the European Court of Auditors' report, just around EUR 2.1 billion in State aid was awarded from 2013 to early 2022 ([75]). Key European players reported total capital investments of about EUR 8 billion between 2013 and 2018, mainly for brownfield capacity expansion.

The first **IPCEI on Microelectronics** was launched in December 2018; it was the very first use of the 2014 IPCEI Communication, justified by the needs to support this sector beyond early R&D, up to first industrial deployment. The IPCEI played a significant role as a policy instrument and has been an important tool in bridging the gap between advanced research and manufacturing, by allowing support until first industrial deployment, and establishing a broad network of collaborations among EU companies. Further, it contributes to **ecosystem growth**, fostering strong **cross-border collaborations** and closer interactions among businesses, academia, startups, and other R&D partners.

The 2018 IPCEI enabled at least **two new greenfield projects**, from Infineon in Villach (AT, EUR 1.6 billion) and Bosch in Dresden (DE, EUR 1 billion). Bosch declared this to be their biggest single investment in the history of the company, which it could make in

([74]) Targeted survey of National authorities. run by PPMI, October-November 2025. Question: "Investment and manufacturing capacity: To what extent do you disagree or agree that EU-level coordination (rather than purely national action) is necessary for achieving EU's semiconductor sovereignty in each of the areas of the Chips pillars?" N=24.

([75]) https://www.eca.europa.eu/ECAPublications/SR-2025-12/SR-2025-12_EN.pdf

Dresden thanks to the IPCEI ([76]). Furthermore, STMicroelectronics built a new 300mm fab in Agrate (IT) and expanded Crolles (FR), while GlobalFoundries (GF) expanded its fab capacity in Dresden for the FDSOI 22nm node. This led to a total of about **EUR 15 billion** private investments in the period 2013-2021, with an average of EUR 2.1 billion per year.

With the Chips Act, the EU has created a dedicated framework for FOAK facilities with the IPF/OEF status and associated guidance, which resulted in a **large surge of investment**: the Commission has approved State aid for eleven FOAK projects to date, with more than **EUR 32 billion** in combined public and private investments, and additional projects are in the pipeline. These projects span advanced logic, power electronics, SiC, FD-SOI, photonics and advanced packaging, and are located across several Member States, signalling a broad strengthening of Europe's industrial base. This means that the level of investments in semiconductors, with an average of EUR 8.5 billion/year, has risen to a level **five times higher than it was before the Chips Act**. The **ESMC** project exemplifies this shift:

> The **European Semiconductor Manufacturing Company (ESMC)** is a joint venture between Taiwan Semiconductor Manufacturing Company (**TSMC**), Robert **Bosch** GmbH, **Infineon** Technologies AG, and **NXP** Semiconductors N.V under the leadership of TSMC. ESMC will manufacture semiconductors on 300 mm wafers with 22–28 and 12–16 nm node sizes. Production will start in late 2027 and reach full capacity in 2029. The project is on track and will boost Europe's resilience by acting as a strategic buffer against semiconductor supply disruptions. In terms of effectiveness, ESMC will likely have a direct impact on EU resilience as it will produce chips in larger node sizes which are mainly demanded by automotive and other industrial users in the European chips market. In addition, ESMC has pledged to prioritize EU and German orders during potential supply crises and will also serve customers beyond its shareholder base, with a strategic focus on European small and medium-sized enterprises (SMEs) and start-ups.
>
> **Public investment triggered by the Chips Act was essential for ESMC**, as such capital-intensive projects depend on substantial and predictable public support. ESMC demonstrates that major semiconductor investments are strategic decisions supported by strong regional innovation ecosystems. Saxony's dense network of research organisations, universities, specialised firms, suppliers and technical labour market reduced investor risk and was decisive in ESMC's location choice. The case underscores that sustained public funding, strong innovation ecosystems, and proactive labour-market measures are all critical for building competitive semiconductor manufacturing capacity in Europe.

Therefore, **overall, the intervention has been effective** in mobilising a higher level of investment. The Commission initially aimed to mobilise **EUR 43 billion** in policy-driven investments in support of the Chips Act up to 2030. Taking into account all components contributing to this target, i.e. public and mobilised funding under Pillar I, national support for Pillar II and the IPCEI on Microelectronics and Communication Technologies, **close to 80% of the envisaged volume** now appears to be committed in roughly **40% of the available time**. This acceleration has been facilitated also by the availability of **RRF resources**, with a number of IPCEIs, first-of-a-kind, and Chips JU projects incorporated into national recovery and resilience plans.

([76]) https://www.bosch-presse.de/pressportal/de/en/come-and-see-the-future-in-dresden-the-new-wafer-fab-is-giving-birth-to-technology-for-tomorrows-world-230016.html

Given that semiconductor manufacturing facilities typically require 2–5 years from ground-breaking to ramping up production, **it is still too early to observe a measurable impact on Europe's effective output capacity** and, consequently, on its global market share. Unfortunately, also decisions beyond the Union's control may have a profound impact, as the Intel case illustrates:

> **Intel's proposed semiconductor fab in Magdeburg, Germany**, was one of the most ambitious European industrial initiatives in recent years, but ultimately never materialised. Announced in March 2022 in the context of the EU Chips Act, the project intended to manufacture chips at 1.5 nm node sizes and thereby establish Europe as the location of one of the world's first sub-2 nm semiconductor fabs. Despite the offer of EUR 10 billion in German federal subsidies, the project was paused in September 2024 and eventually cancelled in July 2025. Between 2023 and 2025, Intel experienced financial pressure marked by operating losses and declining market shares and employee cuttings. These financial strains triggered a strategic reassessment of the project under new CEO Lip-Bu Tan, who was appointed in March 2025. Unlike other Intel fabs, Magdeburg was designed as a foundry-only site, and it was unclear if enough demand would exist for its products. The new CEO shifted from the plan of building up foundry capacity toward a more cautious, demand-driven capacity model. Thus, Magdeburg no longer fitted the revised strategy of Intel. The twin project of a back-end facility in Wrocław, Poland, mainly intended to serve the Magdeburg's production, suffered the same fate. With Intel's manufacturing costs estimated considerably higher than those of competitor TSMC (based on IDC estimates, 1 Euro of capex spent in Taiwan is equivalent to 1.45 Euro spent in the European Union), the company hesitated to establish a leading-edge site in Europe. Moreover, the lack of committed customers for advanced node chips reflects the misalignment between Intel's planned production capacities and Europe's actual semiconductor market and further highlights the need to stimulate industrial demand in advanced node sizes.

In parallel, a **global technology race in semiconductors** has clearly emerged, with the semiconductor industry now treated as a core strategic asset rather than a purely commercial activity. The United States, China, Japan, South Korea and Taiwan – joined by several emerging Asian economies – have all launched ambitious support packages combining large public subsidies, tax credits and regulatory facilitation, pushing worldwide semiconductor investment to unprecedented levels. Therefore, while Pillar II has clearly accelerated the pipeline of large manufacturing projects compared to the pre-Chips Act situation, independent assessments underline that **current investments may be insufficient to close the gap with the US and Asia** ([77]).

Once approved projects become operational, IDC projects that **manufacturing capacity in the Union will increase by more than 38% in absolute terms by 2030**. However, as global capacity is expected to grow at a similar pace, **Europe's share would remain broadly unchanged at around 8%**. Moreover, because this capacity is concentrated in relatively mature technology nodes, its output has lower added value and profit margins than leading-edge logic (such as AI chips). This implies that, even with the same share of capacity, **Europe's share of global semiconductor revenues may actually decline**. Another important aspect is the total value in terms of revenues across the various stages of the semiconductor value chain: a 2024 study from IDC requested by the Commission

([77]) Semi Europe – Chips Act report; https://www.semi.org/sites/semi.org/files/2025-11/SEMI_Chips_Act_Report_Full_Report.pdf

found that because of ongoing investments in other regions, **without the Chips Act Europe's share would have fallen from 8.5% to a mere 5.9%** ([78]).

Another aspect to consider is the **strategic oversight on priority investments**: funding for FOAK manufacturing facilities under Pillar II comes solely from Member States, while the Commission provides only guiding principles for the assessment under State aid rules, not an EU budget for factory incentives. As a result, the Commission can assess State aid and grant IPF/OEF status but has **limited ability to steer a coherent EU investment strategy** (such as prioritising technologies, nodes, or locations) or to avoid resource dispersion and subsidy races. This risks a patchwork of nationally driven projects rather than a coordinated EU-wide manufacturing landscape, weakening long-term strategic coherence.

In addition, although semiconductor equipment is covered by the Chips Act, investment and support remain limited due to a perceived **narrow FOAK definition** ([79]), restricting technologies under Pillar II. Facilities to produce semiconductor manufacturing equipment are within scope of the FOAK definition, but **unclear criteria reduce legal certainty** for potential multi-billion-euro projects, risking delays or cancellations. The same applies to key materials (specialty gases, photoresists, polysilicon). Stakeholders therefore call for stronger support to equipment, materials, and components to reinforce Europe's position in the value chain, sustain technological sovereignty, and reduce vulnerability to supply disruptions ([80]). OPC position papers echo these calls, with stakeholders specifically highlighting the importance of strengthening Europe's PCB manufacturing and back-end processing capabilities to complement front-end investments ([81]).

Recognition of IPF/OEF status

The formal designation in October 2025 of **four major projects as IPF or OEF** (see Section 3.1.2) was a key milestone. These facilities will combine leading-edge process technologies and vertical integration with obligations to support the Union in crisis situations via priority-rated orders. **This directly serves the pillar's core objective of improving security of supply and resilience in the EU**. At the same time, the number of IPF/OEF designations remains modest relative to the size of the European market and the breadth of potential crisis-relevant facilities. In practice, the procedure has been de facto coupled with the granting of State aid; companies believe that they are expected to obtain (or at least apply for) State aid in order to be considered for IPF/OEF status (see example in the text box below), even if this is not the case.

([78]) Contract: CNECT/2022/MVP/0084, "Semiconductors market data by feature size, sector and region", IDC, September 2025.

([79]) Digital Europe, https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/; ZVEI, https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20; ESRA, Position Paper 2025, https://www.esra-org.eu/#documents

([80]) SEMI Europe, https://www.semi.org/en/semi-press-release/semi-europe-publishes-30-recommendations-for-a-forward-looking-european-chips-act; Technology Industries of Finland, https://teknologiateollisuus.fi/wp-content/uploads/2025/10/TIF_Recommendations_EU_Chips_Act_2.0_271025.pdf. Various major industrial companies in documents submitted to the Call for Evidence, not public;

([81]) Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders emphasised value chain completeness. See also the Synopsis report.

In May 2024, a semiconductor manufacturing company submitted an application for the status of IPF under Article 15 of the Chips Act. In this case, the relevant Member State did not, in parallel, notify the intention to give State aid to this company in the context of FOAK. The company wanted to obtain the IPF status to signal to investors the company was a validated European company. At that time, the Commission services deemed that as IPFs should be considered FOAK facilities according to Article 13(2), the company was not able to receive the IPF status, including the rights and obligations associated with the label. This interpretation illustrates the unintended consequences of the intertwined FOAK definition and IPF or OEF, hindering the positive effects of receiving such status.

This coupling helps to align incentives but also explains the relatively small pool of labelled facilities and may limit the coverage of the crisis-response toolbox (priority-rated orders) in the event of a major disruption.

Stakeholder feedback on Pillar II implementation indicates positive early traction: OPC results show that 62% of respondents indicated that Pillar II partially or fully meets its objectives of strengthening security of supply and resilience ([82]). More specifically, 70% of respondents indicated that IPF and OEF facilities partially or fully contribute to security of supply, with supply chain actors showing particularly strong support at 74% ([83]).

Label of design centres of excellence

The "design centres of excellence" introduced in the Chips Act were never operationalised. The label emerged late in the legislative negotiations after co-legislators considered and rejected bringing design activities under the FOAK framework, as design facilities do not face comparable capital-intensive barriers. Instead, the label was added simply to reaffirm that design activities were already eligible under existing RDI State aid rules and to provide a symbolic designation mainly for SMEs or competence centres. Although reflecting the strategic importance of chip design, the label offered no new funding, regulatory advantages, or incentives. Unlike IPF/OEF facilities, which receive practical benefits such as fast permitting, the design-centre label was seen as offering **no meaningful added value**, and implementation work was halted.

As a result, **the label did not strengthen Europe's design ecosystem**: it aligned with policy priorities but provided no usable mechanism, was not applied, and had no impact ([84]). This gap indicates that future revisions of the Chips Act should consider more effective, better-targeted tools to support advanced chip design capabilities.

([82]) Open Public Consultation survey (N=97), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" (60 out of 97 responses: 57% partial + 5% fully). Question: In your view, is the pillar 2 'Security of supply and resilience' of the Chips Act successful in delivering on its objectives?

([83]) Open Public Consultation survey (N=95), data reflecting the percentage of respondents selecting "Fully contribute" or "Partially contribute" (67 out of 95 responses: 46% partial + 24% fully). Question: To what extent are 'integrated production facilities' and 'open EU foundries' contributing to the security of supply of semiconductors and the resilience of the Union's semiconductor ecosystem?

([84]) Digital Europe, https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/

4.1.1.3. Pillar III

Governance – ESB

The ESB's tasks, structure, and operations are of a mainly **technical and advisory role**. In its two years of operation, the ESB has addressed several topics in accordance with its statutory duties (Art. 28) ([85]). It has advised the PAB of the Chips JU on the work programme, the IPF/OEF applications, and on international engagements. However, it has not yet examined other mandated areas (IP rights, confidential information, certification of green/trusted/secure products, or crisis tools). Several Member States have also not submitted complete lists of Key Market Actors due to company-level information challenges.

Because no crisis has been declared, the ESB's crisis-governance effectiveness cannot be fully assessed. Still, a Commission tabletop exercise on supply-chain disruptions showed ESB members responding proactively and cooperatively, demonstrating readiness (see Section 3.1.3) ([86]). The ESB has been particularly effective in tasks outside Article 28, serving as a platform for Commission–Member State coordination on semiconductor policies beyond the Chips Act, including national strategies, cross-border impacts (see Nexperia case below), IPCEIs, and the EU Economic Security Strategy.

Overall, **the ESB functions effectively as a governance body**, with a scope already extending beyond its original mandate. A future Chips Act revision could simplify and broaden its mandate and strengthen horizontal cooperation and information flows among Member States and with the Commission ([87]).

Monitoring and crisis response

The monitoring and crisis response pillar has largely been effective in progressing towards the objective of developing an in-depth understanding of global semiconductor supply chains. Pillar III activities aimed to solve the need for systematic monitoring and crisis response. **The outputs were in fact delivered**: the Commission developed an initial list of early warning indicators, established a strategic mapping framework, and coordinated monitoring and crisis response activities through the ESB. However, there are still steps to be taken towards the operational effectiveness of these outputs.

The consultation showed a **misunderstanding about the roles of the different actors in the monitoring and crisis response activities**. While coordination between the Commission and Member States took place via the ESB (including information on possible disruptions, see the Nexperia case below), most of the outputs were not shared with industrial stakeholders. The reason was both confidentiality matters as well as avoiding creating further fear and uncertainty in the supply chain, which might have a spiralling effect of actually worsening a supply disruption/crisis by triggering an artificial spike in demand.

([85]) Agendas and minutes of all meetings are available at https://ec.europa.eu/transparency/expert-groups-register/screen/expert-groups/consult?lang=en&groupID=3932

([86]) https://digital-strategy.ec.europa.eu/en/news/commission-and-member-states-rehearse-coordinated-response-semiconductor-supply-chain-shortages

([87]) DigitalEurope, https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/

Achieving systematic monitoring, risk preparedness, and crisis response under Pillar III requires further work. Implementation to date shows the **complexity of global semiconductor supply chains**, **limited data availability**, and the **need for action not only by the Commission but also by Member States and industry**. Crisis response also demands **case-specific tools** whose effectiveness is hard to assess without information that becomes accessible only once a crisis is declared. The Commission will therefore continue work through the service contract described in Section 3.1.3.

Monitoring

Monitoring activities delivered strategic-mapping analysis through reports, implemented the SCAN system, and established a semiconductor alert mechanism (see Section 3.1.3). Reports recommended adding specific indicators, as Pillar III monitoring still needs substantial development. "SCAN helps to underpin structural dependencies and to identify early signs of supply chain distress using official data. However, the alert system has been under-used.". Workshop participants noted that monitoring focuses mainly on manufacturers and should extend to distributors and major downstream users, who are critical supply-chain nodes (Workshop 7, 14). National authorities stressed that unclear purposes and use of data discouraged company participation (Workshop 14). Overall, stakeholders view the mechanism as solid but still embryonic.

Despite the EU alert infrastructure, **industry relies on commercial networks for early warnings**. Geopolitical risks and new trade barriers were cited as major operational obstacles, underscoring the importance of monitoring. Yet, only 34% of OPC respondents reported having implemented monitoring systems ([88]). Participants recommended indicators beyond production capacity, covering design, talent, critical materials, and leadership in areas like photonics and quantum technologies (Workshops 7, 13, 14; Workshop 4, 11). This reveals a gap between monitoring's intended focus on disruptions and stakeholders' expectations related to strategic autonomy. Stakeholders also noted uncoordinated, duplicative data requests from Commission services and Member States (Interview 12). Member States described the monitoring framework as complex (Workshop 13).

Crisis response

No crisis stage was activated since the entry into force of the Chips Act. Thus, it is difficult to assess the effectiveness of the crisis response toolbox. The alerts and preventive action phase, leading to the activation of a crisis, was simulated in a tabletop exercise involving the ESB and the Council Working Party on Competitiveness and Growth (Industry) ([89]). The exercise clearly showed the importance for the EU to **increase its preparedness** and to **invest to reduce its dependencies on third countries**. It also showed that **decision-makers need a mandate to collect precise and reliable data** to properly assess supply chain disruptions, even in order to prevent a crisis from materialising.

([88]) Open Public Consultation survey (N=93), data reflecting the percentage of respondents selecting "Yes" to implementation of monitoring systems (32 out of 93 responses). Question: Have you developed or implemented a monitoring system for the semiconductor supply chain in your organization?

([89]) https://digital-strategy.ec.europa.eu/en/news/commission-and-member-states-rehearse-coordinated-response-semiconductor-supply-chain-shortages

For the **crisis toolbox**, stakeholders in consultation workshops noted that the practical steps for using it were not clear enough. The main reason for this is that depending on the crisis, the actual implementation of the tools will largely vary. For example, for a specific crisis, using priority-rated orders (PROs) or common purchasing might not be effective. The Commission will follow up with the implementation with internal work and through the service contract explained in Section 3.1.3.

Nevertheless, it must be noted that **Pillar III's effectiveness is somewhat constrained by limited EU visibility into semiconductor supply chains**, weakening crisis preparedness. Despite improved coordination through the ESB and initial early-warning measures, monitoring remains insufficiently integrated across materials, equipment, design tools, and downstream users. Fragmented and sensitive data further restrict the ability to anticipate disruptions, leaving Pillar III with only partial system-level visibility – a limitation exemplified in the **Nexperia case** presented in the box below.

> On 30 September 2025, the Dutch Minister of Economic Affairs issued an order under its national legislation (the Goods Availability Act) regarding the semiconductor manufacturer Nexperia. Separately, on 1 October 2025, the Amsterdam Enterprise Chamber of Appeal took interim measures related to the company. Shortly afterwards, the Chinese authorities imposed company-specific export control measures on all Nexperia locations in China. This prevented packaging operations performed by Nexperia in China to be re-imported in Europe (i.e., the wafers produced in Europe are shipped to China for low-cost operations of their assembly and packaging into final products – however, these final products could then not be reshipped to Europe, because of the Chinese export control measures taken). Economic operators in the EU and from close partners (including the U.S., Japan) sounded the alarm regarding the licensing process, shipments delays and halts, and the ramifications for downstream industries. The Chinese government eased export restrictions early November. In December 2025, shipments of available chips has continued but uncertainties remain.

4.1.2. Efficiency

The efficiency criterion examines whether the intervention achieved its objectives at reasonable cost and without unnecessary burdens. For the Chips Act, this involves assessing the relationship between resources used (administrative, financial, time) and results achieved (industry uptake, infrastructure deployment, private investment leverage), and identifying unintended cost drivers or duplicative obligations. The analysis considers whether the legislative framework and its implementation were proportionate and streamlined, using cost–benefit analysis, burden-reduction indicators, and comparisons with alternative or baseline scenarios to assess value for money. The overview of benefits and costs presented in Annex III is integrated into the pillar-level analysis below, with Annex III retaining the detailed assumptions and supporting calculations.

As implementation is still at an early stage for several instruments, cost and benefit evidence remains partial and, in some cases, based on indicative estimates (for example standard cost model assumptions for administrative burden). In Pillar II, operating cost data for new fabs are not yet available and some total investment figures are not disclosed, whilst in Pillar III the costs and burdens of crisis measures are inherently uncertain because no crisis stage has been declared. Accordingly, efficiency findings in this section should be read as an initial assessment grounded in available evidence, avoiding conclusions that cannot yet be robustly substantiated.

In the following subsections, efficiency will be examined pillar by pillar, focusing on whether resources were proportionate to results and whether implementation generated avoidable costs or administrative burdens.

4.1.2.1. Pillar I

Pillar I demonstrates **strong efficiency in resource mobilisation and financial leverage**, with instruments delivering substantial outputs relative to inputs. In financial terms, as of November 2025, total EU-level public expenditure committed under Pillar I is around EUR 1,960.5 million (EUR 1,831.2 million for pilot lines, EUR 92.3 million for competence centres, EUR 25 million for the Design Platform, and EUR 12 million for design-related activities), whilst national public expenditure stands at roughly EUR 1,957.3 million for pilot lines and competence centres, broadly matching EU contributions. The most striking efficiency achievement is the approximately 1:1 leverage ratio between EU contributions and national funding for pilot lines, competence centres, and quantum chip pilots. This is particularly remarkable for the case of the competence centres, which prompted an unprecedented EU-wide mobilisation, with all Member States, including those that had never engaged in JU activities, participating and providing funding. Additionally, the Chips JU achieved strong administrative cost-effectiveness in 2023, with total administrative costs representing just 1.09% of operational expenditure, comparing favourably to benchmarks for similar Joint Undertakings.

Beyond financial leverage, market uptake provides complementary evidence of **efficient resource targeting**. The Chips Fund demonstrated strong demand, with the EIC Accelerator thematic allocation fully deployed in less than two years. This strong uptake occurred within the context of a EUR 300 million EIC allocation and EUR 250 million InvestEU dedicated capacity for semiconductors, validating that the well-documented European venture capital gap for semiconductor startups persists and that demand substantially exceeds available resources. By relying on existing instruments and governance structures, notably the EIC Accelerator (both thematic and open calls), the STEP programme and the InvestEU/EIF framework, the Chips Fund has leveraged established procedures, expertise and synergies. In cost terms, the Chips Fund adds EUR 425 million in EU contribution: EUR 300 million via the EIC Accelerator (EUR 62 million in grants and EUR 238 million in recommended equity investment to 24 startups through the dedicated Semiconductor and Quantum Technologies challenges) and EUR 125 million via InvestEU (EUR 68 million signed or approved with four financial partners, resulting in EUR 116 million in equity investment to 31 companies)

The Chips Fund is designed to crowd in private investments with a leverage factor of 3 to 5. This strongly suggests that objectives have been pursued at a reasonable cost for the EU budget and with limited additional administrative burden for both the institutions and beneficiaries. Available burden estimates indicate that administrative effort is nonetheless material for applicants: a standard cost model suggests an average of around 70 person-days per Chips Fund beneficiary for applications, due diligence and reporting (about EUR 30,000 per funded project, excluding costs for unsuccessful applicants), whilst across Pillar I grants an estimated 10-20 person-days per application (midpoint 15 days) implies around EUR 3 million in administrative and compliance costs for 514 participants in 44 projects over four years (indicative).

At the same time, the **strong demand and rapid budget consumption of the Chips Fund** suggest a highly competitive environment, which can be seen as efficient in terms

of selection quality, but also implies that **many worthy projects remain unfunded**. This underlines that the main constraint is budgetary rather than operational inefficiency. Overall, taking into account leverage effects of private funding, use of existing structures, and the absence of obvious deadweight or underuse, the intervention appears to have delivered its early objectives at a reasonable cost and without evident resource wastage. At this stage, the efficiency assessment is also supported by early output evidence reported elsewhere in the evaluation (for example the operationalisation of pilot lines and competence centres), although full cost-effectiveness will depend on sustained utilisation rates and longer-term outcomes.

Deployment timelines varied across Pillar I components, but generally demonstrate satisfactory efficiency given the scale and institutional novelty of the instruments involved. Pilot lines – which are complex cross-border technology infrastructures with substantial equipment procurement requiring coordination across multiple Member States – progressed from call launch to grant agreement signing within just ten months. Competence centres achieved operational status across 28 countries within timeframes stakeholders described as reasonable (workshop 14). The Design Platform experienced notably longer implementation timelines due to structural complexity and a novel cloud-based virtual infrastructure, though these extended timescales remain proportionate to the scope and ambition of establishing fundamentally new European capacities in design. For quantum chip pilots, six Framework Partnership Agreements have been signed without financial commitment, with first commitments expected at the beginning of 2026, which limits the extent to which cost-effectiveness can be evidenced at this stage beyond readiness.

Whilst the fundamental structure of separate funding programmes under the current MFF cannot be easily altered, **improved guidance and harmonised timelines** could reduce administrative burden. The efficiency gains from such procedural improvements would benefit all stakeholder groups, with proportionally larger benefits for SMEs and academic actors facing higher relative coordination costs.

4.1.2.2. Pillar II

As explained in Section 3.1.2, Pillar II of the Chips Act has made significant strides in **mobilising substantial resources to enhance Europe's semiconductor capabilities**. The mobilisation of over EUR 80 billion in investments, including under an IPCEI and of Pillar II, demonstrates the Act's capacity to attract large-scale financing and support the objective of expanding Europe's semiconductor production base. OPC results show that 62% of respondents indicated that Pillar II of the Chips Act was (partially or fully) successful in delivering on its objectives (see Section 4.1.1.2), and that 71% of respondents agreed partially or fully that the Chips Act Pillar II has made the EU a more attractive location for semiconductor manufacturing) ([90]).

The administrative burden of **prolonged approval processes** has emerged as a significant challenge in Pillar II's implementation ([91]). The extensive timelines for

([90]) Open Public Consultation survey (N=96), data reflecting the percentage of respondents selecting "Fully" or "Partially" (69 out of 96 responses: 61% partial + 10% fully). Question: To what extent had the European Chips Act Pillar 2 on security of supply and resilience, made the EU a more attractive location for semiconductor manufacturing?

([91]) ZVEI, https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20

permitting approvals have become a substantial cost factor, particularly in comparison to other more efficient systems. For example, Interview 5 with industry representatives states that **while State aid approval in the EU takes 10-12 months** ([92])**, the same procedure takes 6 months in South Korea and Taiwan, and even less than one month in other regions**. Nevertheless, in the case of IPF/OEF the Commission increased the procedural efficiency of the intervention with the publication of guidelines ([93]). Whilst direct EU-level financial costs are limited (public investments are made by Member States and the EU role is largely regulatory and supervisory), these time costs can materially affect overall efficiency by delaying delivery and increasing financing and opportunity costs for capital-intensive projects.

Efficiency achievements in Pillar II are mainly impacted by **fragmented coordination across the EU, national, and industrial stakeholders**. Certain stakeholders have pointed out some inefficiencies in the administrative processes, such as extended timelines for State aid approvals (Workshops 4 and 9). Potential changes in the administrative procedures could be envisaged. Some stakeholders present at Workshop 4 as well as ESIA, ZVEI and DigitalEurope ([94]) propose the establishment of a centralised EU semiconductors budget (inspired by the Draghi report) that could unify decision-making and expedite strategic investments and give 'top ups' in IPCEIs and FOAK projects. Budget dedicated to semiconductors under the upcoming European Competitiveness Fund (ECF) would enable fast funding for highly strategic projects ([95]). Indicative administrative-cost estimates for the State aid lifecycle suggest recurring compliance and processing effort for firms and administrations (for example, stylised estimates of around 50 person-days per beneficiary per year for firms and comparable order-of-magnitude effort for EU and national authorities), but the evidence base remains incomplete and does not capture operating costs of new facilities, which are not yet available.

Another element that affects the implementations efficiency is the **limited staffing and resources** dedicated to the implementation of the Chips Act (around 20 Commission staff, as compared to initially around 120 staff in the American CHIPS Act office). Nevertheless, the interaction between the Commission and notifying parties reflects efforts to enhance coordination and technical rigour. For both FOAK and IPCEI cases, DG COMP and DG CNECT work in close coordination; the former engaging in discussions with Member States during pre-notification and notification stages whilst the latter provides technical assessment and evaluation of spillover effects.

([92]) Ibidem and Interview 5

([93]) Communication (C/2024/4911) from the Commission on the Guidance on the application for an undertaking to obtain the status of integrated production facility and open EU foundry pursuant to Article 15 of the Chips Act Regulation (EU) 2023/1781

([94]) ESIA, https://www.eusemiconductors.eu/sites/default/files/2025.09.12_ESIA-Position_EUChipsAct2.pdf; ZVEI, https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20; DigitalEurope, https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/

([95]) Semi Europe, https://www.semi.org/sites/semi.org/files/2025-11/SEMI_Chips_Act_Report_Full_Report.pdf

4.1.2.3. Pillar III

Pillar III's efficiency is shaped by a paradox: its value lies in preparedness even when its tools are never used ([96]). Because no crisis has been declared, **assessing the efficiency of this pillar can only be done with inherent limitations**. In cost terms, Pillar III currently entails modest running costs linked to monitoring and coordination: indicative estimates suggest annual business compliance costs of around EUR 0.6 million (around 50 firms each spending roughly 160 hours per year), EU-level monitoring costs of around EUR 1.5 million (including FTE and analytical support), and national administrative costs of around EUR 1.5 million in total across Member States (modelled).

The ESB's set-up and Commission-led coordination have been proportionate to the value created. It has provided a plenary forum for Member States to exchange views and has spawned expert groups such as the situational-analysis taskforce ([97]) facilitating more agile workflows. The ESB was established on time and within its expected cost. However, given that several crisis-stage tools have not been activated, this proportionality finding should be treated as an initial assessment focused on preparedness outputs rather than a definitive judgement on cost-effectiveness.

A recurring recommendation is to **strengthen exchanges between the ESB and industry** (Workshop 7, ESIA), reflecting the incomplete implementation of an anticipated high-level industry body. This dialogue could improve once the Steering Committee foreseen in the Terms of Reference for the Industrial Alliance is established. A first step has been the formation of a high-level Industry Advisory Group as a subgroup of the Industrial Alliance which will produce in March 2026 a report on industry priorities for the Chips Act revision before transitioning into the foreseen Steering Committee of the Alliance. Even so, bringing together experts from all Member States and observers has helped build relationships, improve information flows, and support consultations. From an efficiency perspective, more structured industry exchange is also relevant to keeping monitoring requests proportionate and reducing duplication, thereby limiting compliance costs.

Furthermore, the Commission is **using the ESB to develop crisis coordination mechanisms** in close collaboration with the Member States to enable the Union to react to crises. To increase the coordination efficiency and clarify the roles of different actors, the Commission organised a tabletop exercise on coordinated response to a semiconductor supply chain crisis (see Section 3.1.3).

At the same time, the Commission-internal organisation of the obtained data to glean insights in times of crisis has not been tested yet. However, pre-crisis stage supply chain challenges (see Nexperia case in Section 4.1.1.3) have shown that not only the Member States but also the Commission are facing **challenges regarding their ability to obtain and work with data in a more timely and efficient manner**. Similarly, Workshop 7 participants reported that the lack of a shared platform to monitor semiconductor value

([96]) Assessment in this subsection is based on Workshop 7, Workshop 3, ESIA, and the European Economic and Social Committee.

([97]) The Task Force on Situational Analysis is a subgroup of the European Semiconductor Board composed of a small number of experts volunteered by 6 Member States. It assists the Commission in the collection and analysis of evidence regarding rapidly developing situations or imminent risks to economic security in the field of semiconductors, when coordinating 27 Members would be too slow.

chains across Europe creates challenges for EU crisis preparedness. At the same time, companies report that they **remain cautious about sharing supply chain information** due to competition concerns, complicating data aggregation and sharing whilst protecting sensitive information. Increasing the administrative abilities of the Commission to request and handle data in a preventive stage would save time and resources should a crisis occur since the necessary time and caution in establishing the tools would pre-empt failures in an ad hoc set-up during a crisis. This also has a direct efficiency implication: improving data-handling processes and confidentiality safeguards in the preventive stage can reduce the risk of costly, duplicative or low-quality data collection during a crisis.

Finally, industry representatives express concern that the **crisis-toolbox measures could impose heavy administrative burdens**. However, these tools are intended for use only in critical situations, where such burdens would be justified and applied solely when necessary and proportionate to keep essential sectors functioning. Since these measures have not been used, their administrative and opportunity costs remain prospective and should not be treated as observed efficiency outcomes at this stage of implementation.

4.1.3. Coherence

This section assesses the coherence of the Chips Act internally, across its three pillars, and externally, in relation to other EU initiatives, Member State actions, and wider EU policy priorities.

4.1.3.1. Internal coherence across the three pillars

The Chips Act is structured around three interlinked pillars that were designed to operate as a single policy pipeline, connecting upstream research and development (Pillar I), industrial deployment (Pillar II), and crisis preparedness (Pillar III). Governance arrangements through the ESB were designed to ensure coherence across the three pillars, including through common oversight and coordinated crisis response.

From a conceptual perspective, **the pillars are coherent and mutually reinforcing**. Pillar I is intended to generate the research and development outputs that could become the bases for manufacturing investments under Pillar II, while Pillar III protects both through monitoring and emergency measures. This architecture was explicitly conceived to address the structural gap between publicly funded research and industrial deployment.

4.1.3.2. External coherence with EU, national, and regional initiatives

Coherence with EU initiatives

The Chips Act is broadly coherent with EU initiatives pursuing similar objectives, notably the Digital Europe Programme (DEP), Horizon Europe (HE), the Critical Raw Materials Act (CRMA), but also European Regional Development Fund (ERDF), European Social Fund Plus (ESF+), Connecting Europe Facility (CEF), InvestEU, Erasmus+ and the Recovery and Resilience Facility (RRF). This is confirmed by policy-document analysis and stakeholder consultation. From the abovementioned initiatives, the Chips Act is particularly coherent with DEP and HE, which serve as the two funding backbones of Pillar I. **DEP** provides horizontal digital infrastructures, while **HE** supports upstream research, piloting and demonstration. Moreover, the Act is also complementary

to the **CRMA** ([98]), as both pursue strategic autonomy by addressing different segments of the value chain: the Chips Act focuses on semiconductor design and manufacturing, while CRMA targets critical raw materials.

InvestEU provides part of the financing backbone of the Chips Fund, bridging the gap between grants and commercial investment. Stakeholders noted navigation difficulties between the Chips Fund and EIC support mechanisms (Workshop 14), indicating practical coherence issues in funding access. Coherence with **IPCEIs**, namely IPCEI ME/CT, is high. IPCEIs continue to support high-risk cross-border R&D and first industrial deployment, while the Chips Act complements this through permanent capacity building and resilience mechanisms. Stakeholders confirmed alignment and synergies between the two instruments (Interviews 1, 6 and 9). When it comes to the EU programmes listed in Annex III of the Chips Act, there is a broad coherence with ERDF, ESF+, CEF, Erasmus+ and the Recovery and Resilience Facility (RRF). These instruments support complementary parts of the value chain, from regional financing to skills.

Coordination will be needed between the Chips Act and the proposed **European Competitiveness Fund** (ECF) or the upcoming **Quantum Act**. Coherence with the latter will provide an opportunity to establish a comprehensive European quantum policy frameworks that leverages synergies across multiple instruments.

The Chips Act is coherent with the EU's **strategic autonomy, economic security, and competitiveness agendas**. It aligns with the European Economic Security Strategy, Dual-Use export controls, the Foreign Subsidies Regulation, and the Strategic Technologies for Europe Platform (STEP). Together, these instruments reduce strategic dependencies and reinforce industrial capacity. The Act is coherent with EU competition and industrial strategy, as reflected in industrial strategies and the Draghi Report, and it complements digital and green frameworks.

Coherence with national initiatives

At national level, coherence is generally high. Policy reviews confirm that national strategies in Germany, France, the Netherlands, Portugal, Ireland, Finland and Czechia explicitly refer to the Chips Act and align governance structures and co-financing instruments. The importance stakeholders place on coordination is reflected in OPC results: 86% of respondents indicated that the Chips Act has contributed adequately, well, or very well to increasing governance and coordination between national and regional authorities and agencies ([99]).

Furthermore, stakeholder feedback indicates broad recognition that **strengthened coordination is necessary**. OPC results show that 88% of respondents agreed that dispersed national strategies require EU-level coordination to ensure Member States

([98]) https://eur-lex.europa.eu/eli/reg/2024/1252/oj/eng

([99]) Open Public Consultation survey (N=67), data reflecting percentage of respondents rating coordination as "Adequately", "Well", or "Very well" (58 out of 67 responses: 61% adequately + 16% well + 9% very well). Question: To what extent has the Chips Act contributed to increase the governance and coordination between different national and regional authorities and agencies?

contribute efficiently and coherently to strengthening the semiconductor value chain ([100]). This strong consensus validates the Act's coordinated governance approach.

Coherence with regional initiatives

At regional level, regional stakeholders reported limited inclusion in governance processes and limited involvement in implementation. However, it is important to note that the reasons for fragmentation go beyond the scope of the Chips Act. Workshop 4 with the European Semiconductor Regions Alliance (ESRA) ([101]) showed that the Chips Act has in many cases strengthened and empowered the regional industrial policies of regions with a background in semiconductors, and that it offered unique opportunities by complementing existing national and EU instruments. In fact, ESRA credits its own creation, and its work on exchanging good practices and representing regional instances, to the political impulse given by the Chips Act. OPC position papers from regional stakeholders further emphasise opportunities to strengthen multi-level coordination, noting that success depends on close collaboration between research, companies, pilot lines, centres of excellence, and public policy at all governance levels ([102]).

4.2. How did the EU intervention make a difference and to whom?

4.2.1. EU added value

This criterion assesses the EU added value of the Chips Act. Because semiconductor value chains are cross-border and no Member State is self-sufficient, **EU action aims to avoid duplication, achieve scale, and coordinate investments**. The assessment examines how effectively the Act has pooled resources, aligned priorities, strengthened cooperation, reduced fragmentation, and improved the EU's collective capacity to face global competition and supply-chain risks, delivering benefits beyond national initiatives.

4.2.1.1. Pillar I

Pillar I has created **transnational infrastructures beyond the reach of individual Member States**, offering pan-European access to five pilot lines and six quantum chip pilots across 13 countries. This avoids redundancy, ensures broad technological coverage, and enables efficient prototype production. Without the EU framework, Member States would face costly, duplicative investments with low utilisation, while smaller countries would lack access to advanced facilities. The design platform and competence centres further support cross-border expertise sharing.

OPC results strongly confirm this EU added value: 70% of respondents agreed Pillar I increased EU competitiveness through enhanced design, systems integration, and

([100]) Open Public Consultation survey (N=94), data reflecting percentage of respondents selecting "Strongly agree" or "Agree" (83 out of 94 responses: 38% strongly agree + 50% agree). Question: Do you agree with the following statement: "Dispersed national strategies require EU-level coordination strategies to ensure that Member States contribute efficiently to the strengthening of the EU's semiconductor value chain in a coherent and complementary fashion."

([101]) https://www.esra-org.eu/

([102]) Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Regional stakeholders highlighted coordination opportunities. See also the Synopsis report.

production capabilities, and 78% agreed it enabled the development and deployment of cutting-edge semiconductor and quantum technologies ([103]).

4.2.1.2. Pillar II

The EU added value of Pillar II lays in **de-risking large-scale investments in compliance with State aid rules** and allowing for **faster national permitting procedures**. The Chips Act Communication explains the principles for the case-by-case assessment of State aid measures supporting new semiconductor manufacturing facilities directly under Article 107(3)(c) TFEU. In particular, the Commission may take into account the fact that projects are FOAK in the EU and will verify that the aid does not exceed the project's funding gap (taking into account the counterfactual scenario in the absence of aid when relevant). Such case-by-case assessment of manufacturing aid directly under the Treaty is exceptional as manufacturing aid is typically only allowed in assisted regions. These measures under Pillar II complement support measures for R&D&I activities and IPCEI projects up to first industrial deployment, where projects have to demonstrate their uniqueness at global level. Coordination sought to prevent a subsidy race among Member States while creating spillovers and conditions attractive enough to compete globally for semiconductor manufacturing capacity. Moreover, the EU added value of IPF/OEF facilities mainly lies in their commitment to accept and prioritise crisis-relevant orders in times of crisis.

However, Pillar II gives the Commission **limited tools at the EU level for steering manufacturing investments**, since public support mainly comes from Member States. As a result, investments have naturally developed in a decentralized manner, with firms often choosing locations based on national funding conditions rather than broader EU strategies, possibly impacting efforts to address value chain gaps at the Union level.

4.2.1.3. Pillar III

Under Pillar III, the ESB was created to coordinate monitoring, risk preparedness, and crisis response at the EU level, a feat not possible at the national level due to fragmented priorities. The ESB lowers transaction costs and enhances communication across Member States, providing distinct EU-level value. It strengthens economic security for all, including smaller Member States less involved in the semiconductor industry, by providing resilience and insights into the value chain. The ESB offers agility for quick, coordinated action during disruptions and serves as a point of contact for industry stakeholders. Through crisis response tools, the ESB enhances collective Member State action, providing EU-added value. These efforts streamline responses to crises, minimizing fragmentation risks and securing Europe's economic stability. Coordinated EU-level action was strongly supported by the OPC results: 88% of respondents agreed or strongly agreed that dispersed national strategies require stronger EU-level coordination to ensure Member States contribute coherently to the semiconductor value chain, and only 2% disagreed (see footnote 100). The targeted survey results also show

([103]) Open public consultation survey (N=96), data reflecting the percentage of respondents selecting "Fully meets the objectives" or "Partially meets the objectives" to Question Q6. To what extent does pillar 1 'Chips for Europe Initiative' of the Chips Act deliver on its objectives? Options: "To reinforce advanced design, systems integration and chip production capabilities in the Union, thereby increasing the competitiveness of the Union" and "To enable development and deployment of cutting-edge semiconductor technologies, next-generation semiconductor technologies and cutting-edge quantum technologies and the innovation of established technologies".

high level of agreement on the need for EU-level coordination in order to achieve sovereignty for the EU in semiconductors (ranging 75-86 % depending on stakeholder group). OPC position papers similarly call for strengthened international partnerships with key semiconductor-producing nations, proposing more formalised cooperation mechanisms and risk-based frameworks to enhance Europe's global semiconductor collaboration ([104]).

4.3. Is the intervention still relevant?

4.3.1. Relevance

The relevance criterion assesses whether the Chips Act's objectives and intervention logic **remain suited** to current needs, technological developments, market conditions, and geopolitical realities. It examines whether the Act still addresses its original problems, how these have evolved, and whether new challenges have emerged. It also evaluates whether the Act's instruments align with stakeholder needs across the value chain and whether any gaps or new priorities exist.

4.3.1.1. Pillar I

Pillar I addresses fundamental capability gaps in the EU semiconductor ecosystem that have become even more urgent since the Chips Act's adoption. The strategic relevance must be **assessed against the counterfactual situation**: without the Chips Act, the EU would possess only the KDT Joint Undertaking supporting bottom-up research projects without political steering or strategic coordination. The entire architecture that Pillar I has established would simply not exist.

The response of Member States in developing **national semiconductor strategies** shaped by the Chips Act provides tangible evidence that the intervention corresponds to genuine needs at both national and European levels. In several cases, parts of the Chips Act structure are often directly mirrored in national strategies, demonstrating alignment between European intervention and Member State priorities. For many Member States, competence centres represent the first engagement with semiconductor policy, catalysing strategic thinking and capacity development that would not have occurred without EU-level framework and co-funding.

Pilot lines translate EU research excellence into industrial deployment. The lab-to-fab gap persists as a major drawback for the EU semiconductor sector despite our excellence in R&D, with fragmentation across the EU reducing the speed and impact of technology transfer. The EU's strengths in research and technology organisations allow for industrial-scale prototyping infrastructure to enable technology transfer, a need that has not diminished since the Chips Act's adoption. Pilot line relevance is evidenced by the strong demand received, in the form of industry access requests, even before their official launch. However, survey evidence suggests that structural barriers to technology transfer persist: nearly half of RTO respondents (47%, 8 of 17) reported significant barriers to transferring research results into industrial application. R&I alone cannot secure

([104]) Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025. Stakeholders provided recommendations for international cooperation frameworks. See also the Synopsis report.

European competitiveness without complementary manufacturing capacity, identifying gaps in packaging, substrates, PCB production and system-integration activities (Workshops 7, 8 and 11, Interviews 8, 11; position paper – Global Electronics Association ([105])).

The Design Platform addresses the EU's weakness in chip design capabilities, where the continent lags behind global competitors despite strong electronics and systems integration sectors. Technological trends such as AI accelerators, chiplet architectures, and power semiconductors increasingly shape industrial priorities, intensifying demand for design expertise. Since 2023, market growth has been increasingly driven by AI-related applications, particularly processors and memory for data centres, reinforcing the strategic relevance of strengthening leading-edge design and integration capabilities in the Union. Despite ongoing efforts, the Europe's design deficit persists, and EU-level intervention remains necessary to close capability gaps that national programmes have not resolved (workshop 14).

Competence centres continue to be relevant thanks to their semiconductor-focused activities across all Member States. This unprecedented geographical reach addresses national/regional capability building and SME access that national programmes alone could not achieve given the concentration of semiconductor expertise in some Member States. Just like shared pilot lines expanded access to advanced prototyping capability, competence centres have strengthened collaboration and training (Workshops 3, 5 and Interview 7). A *Coordination and Support Action* ensures knowledge sharing among competence centres rather than isolated national efforts. Given that most competence centres only began operations in 2025, their longer-term impacts on technological capability and competitiveness cannot yet be evidenced, but early outputs indicate strong alignment with identified needs.

Skills emerged as a cross-cutting constraint ([106]): stakeholders across design, R&I, manufacturing, packaging, automotive, telecoms and materials reported persistent shortages in applied semiconductor engineering, packaging and system-integration skills. The OPC results confirm this: the majority of respondents (94%) fully agreed or agreed that the European semiconductor industry faces serious talent shortages, posing a major bottleneck for growth and innovation, which requires investment in attraction, skilling, reskilling, and training policies ([107]).

Workshop 14 with the Chips JU Public Authorities Board emphasised that long-term vision and continuity should take priority over launching new initiatives. National authorities stressed that sustained commitment to existing instruments creates essential consistency for extended development processes that are characteristic for semiconductor technology. Pillar I remains highly relevant to address the persistent capability gaps that require European-level action. These are design weaknesses, lab-to-fab gaps, fragmented competence centres and insufficient venture capital. Addressing our capability gaps is

([105]) Global Electronics Association, https://emails.ipc.org/links/GlobalElectronicsAssocChipsActPlusPosition.pdf

([106]) European Semiconductor Regions Alliance, Position Paper 2025, https://www.esra-org.eu/#documents

([107]) Open public consultation survey (N=94), data reflecting the percentage of respondents selecting "Strongly agree" or "Agree" (89 out of 94 responses). Question: Do you agree with the statement that the European semiconductor industry faces serious talent shortages requiring investment in attraction, skilling, reskilling and training policies?

even more urgent given intensifying global competition and geopolitical technology dynamics.

4.3.1.2. Pillar II

This section assesses whether Pillar II remains aligned with Europe's evolving industrial needs. Stakeholders have confirmed the relevance of the Chips Act's core objectives of reinforcing domestic manufacturing capacity and reducing strategic dependencies. Data from the OPC supports that IPFs/OEFs partially or fully contribute to the security of supply of semiconductors and the resilience of the Union's semiconductor ecosystem (see footnote 83). However, many considered the original design to be increasingly misaligned with current vulnerabilities, as it was perceived as focusing primarily on front-end fabrication while overlooking dependencies in substrates, specialty chemicals, advanced packaging, RF and power modules, PCBs and EMS (Workshops 2, 7, 9, 11; Interviews 8, 9, 10).

Several stakeholders argued that maintaining minimum viable capacity and skills had become more relevant than achieving a global 20% market share (Workshops 10, 11, 15), pointing to a growing mismatch between Pillar II indicators and industrial realities ([108]). OPC position papers validate this perspective, with industry stakeholders emphasising that production capabilities must be accompanied by framework conditions that support end-market development for semiconductors made in the EU ([109]).

Finally, stakeholders identified weak domestic demand as a growing constraint that is specific to advanced-node production ([110]). While global demand for semiconductors remains strong, market leaders nowadays tend to locate cutting-edge fabrication where sustained local demand exists, as production follows demand. In case of a severe crisis, for instance an earthquake destroying advanced production facilities on Taiwan, it is very likely that countries will limit domestic production for domestic consumption via export controls and other measures. Considering potential exposure during crises, and to reduce their dependencies on other parts of the world, countries such as the United States and Japan have invited the world leader in advanced nodes manufacturing, TSMC, to set up advanced node facilities on their soil. Thanks to sufficient local demand, TSMC agreed to do so.

The Union remains dependent on third countries for advanced-node manufacturing capacity. In the event of a severe supply-chain disruption or geopolitical crisis, export controls or prioritisation of domestic markets could limit EU access to such production. In case of a crisis, the Union may be faced with a situation where its industries do not have the possibility to access advanced nodes production. Demand side measures, such as demand aggregation, may therefore be needed to put in place sufficient local demand to convince market leaders to establish advanced production facilities in the Union and/or to justify public-private investments in small-scale advanced nodes production in Europe.

([108]) This is echoed by DigitalEurope, who states that "Europe's next targets must reflect strategic relevance, not production quotas", https://www.digitaleurope.org/resources/chips-act-2-0-from-emergency-response-to-strategic-industry-development/

([109]) Position papers submitted to the consolidated public consultation of the review of the Chips Act, September–November 2025, including contributions from ASML and other industry stakeholders. See also the Synopsis report.

([110]) ZVEI, https://www.zvei.org/en/press-media/publications/towards-a-european-chips-act-20

In this context, such demand-side measures were considered relevant to anchor advanced production capacity in the Union and reduce strategic dependency (Workshops 4, 10, 12; Interviews 2, 3, 11). A public-sector investor further warned that without credible demand projections and production baselines, monitoring and crisis-response mechanisms under Pillar III risk being weakened, as they depend on realistic assumptions about available capacity (Interview 2).

These considerations suggest that Pillar II remains relevant to Europe's industrial objectives, but that its original focus and performance indicators may not fully reflect evolving technological and geopolitical realities.

4.3.1.3. Pillar III

Pillar III's focus on systematic monitoring, risk preparedness and crisis response remains relevant, as supply chain dependencies persist. Geopolitical tensions, trade restrictions, export-control regimes and subsidy competition have further increased the strategic importance of systematic monitoring and preparedness mechanisms. Supply chains have become instruments of economic security policy, heightening the relevance of coordinated EU-level action. As discussed in Section 3.2, global value chains have changed dramatically. Therefore, European companies dependent on semiconductors have reported early improvements in coordination that may support risk mitigation through the Chips Act, but they are now exposed to new challenges caused by drastic changes in global markets.

Economic security and digital sovereignty have gained relevance in the Commission's overall policy goals, pointing to the increased importance of resilient semiconductor ecosystems. Moreover, **the necessity of ex-ante risk preparedness as opposed to ex-post crisis response has increased in light of unforeseen supply chain disruptions** (see Nexperia case in Section 4.1.1.3). Pillar III mechanisms improved information exchange and crisis coordination (Workshops 6, 14, 15); however, given the short implementation period, impacts on actual resilience or crisis mitigation capacity cannot yet be evidenced. The Commission was largely successful in addressing the needs for improved visibility of supply-chain risks of public authorities and large industrial actors (Workshops 6, 14, 15; Interviews 1, 4). Nevertheless, crisis preparedness can only be achieved through **cross-pillar interventions and multi-stakeholder actions** between the Member States, the Commission and the private sector. In light of intensified geopolitical tensions and supply-chain weaponisation, the Chips Act may contribute to mitigating certain risks, but cannot fully address all emerging vulnerabilities.

Scope is key in assessing the relevance of Pillar III, both within the semiconductor value chain and the European Union. Crisis response mechanisms protect all Member States, not just those with production capacity. Many EU industries rely on the same semiconductors and product flows within the Single Market. This makes the Pillar III mechanisms being embedded in the ESB, with full Member States representation, relevant. As OPC results demonstrate, most stakeholders are either uninvolved with and do not know the extent to which Pillar III delivers on its objectives (40%) or believe it did not meet its objectives (30%) ([111]).

([111]) Open public consultation survey (N=96), data reflecting the percentage of respondents selecting "Don't know / Not involved" or "Does not meet the objectives" (67 out of 96) for the question: Q18.

Consultations suggest that, to capture system-wide risks, the scope of crisis response mechanisms needs to be extended to cover base materials, substrates, materials, packaging, assembly, downstream electronics, and end-user industries. Not including these elements allows vulnerabilities in the value chain to go unnoticed, limiting the relevance of crisis response for downstream and end-user sectors, and eventually customers (Workshops 7,9,11; Interviews 8, 10). The PCB assembly and EMS industries seek inclusion and argue that a wider approach to risk mitigation can help identify risk patterns more effectively (Workshops 6, 7, 9, 11, 14, 15; Interview 1, 4, 8, 10).

To what extent does Pillar 3 (Monitoring and crisis response) of the Chips Act deliver on its objectives?

5. WHAT ARE THE CONCLUSIONS AND LESSONS LEARNED?

5.1. Conclusions

This evaluation concludes that **the Chips Act has been key in establishing a European semiconductor regulatory and policy framework** that did not previously exist and did so in a short period of time. It mobilised substantial public and private investment, introduced state-of-the-art EU-level infrastructures, and put in place governance mechanisms for coordination and crisis preparedness. Stakeholder confidence in the overall strategic direction remains high, and the Act is widely perceived as a necessary response to geopolitical, technological, and economic pressures.

At the same time, **the transition from output delivery to system-wide results and impacts is still ongoing**. The main constraints are structural and economic rather than operational and relate to the Union's ability to industrialise innovation, finance scale-ups, reinforce supply chain resilience, and generate system-level intelligence.

The Act has been **instrumental in building technology infrastructures and early-stage manufacturing capacity**. The creation of EU-level pilot lines, competence centres and shared infrastructures has ensured coordinated effort. Such initiatives are already improving access to advanced tools and support a strong cross-border collaboration. The impact of other components (namely, quantum chip pilots and the design platform) will only become apparent at a later stage. In any case, stakeholders widely recognise the Act's contribution to strengthening Europe's R&I base and improving coordination across Member States.

By contrast, **progress in manufacturing deployment and subsequent increased strategic autonomy is still at an early stage**, partly due to long lead times between investment decisions and actual production in fabs. Europe remains structurally dependent on non-EU suppliers in critical segments, particularly at advanced technology nodes, and the loss or delay of major investment projects demonstrates that sovereignty has not yet materially improved.

Across the evaluation criteria, **the lab-to-fab gap emerges as an important challenge**. The Act has already managed to move technologies to higher readiness levels and – considering the short time since its entry into force – stable pathways to volume manufacturing are expected to materialise in the coming years. Many outputs operate effectively at a technical level and will generate the industrial capacities required to secure European supply later in time. The challenge confronting the EU is no longer primarily innovation generation, but **industrialisation and scale**.

The evaluation also finds that **limited private capital continues to limit the scaling of European semiconductor firms**. While the Act mobilised unprecedented levels of public funding, private investment (particularly, late-stage and institutional) remains insufficient compared to competing regions. Support for scale-ups is constrained by structural features of the European financial system, including the lack of a real Capital Market Union, existing rules for pension funds, and conservative investment practices. This weakens European value capture and incentivises scale-ups to relocate or get acquired by non-EU firms. The Act has improved early-stage innovation capacity, but the allocated budget to the (EIC Accelerator part of the) Chips Fund, consumed in its first two years, has proven insufficient. Thematic instruments with patient capital are necessary to help semiconductor startups in scaling up and broader measures must be conceived to create the conditions required for industrial 'champions' to emerge.

In addition, the evaluation finds that current **EU-level instruments to address security of supply and economic security vulnerabilities are useful tools, but should be further strengthened**. On the one hand, manufacturing deployment is shaped primarily by industry investment decisions supported through national funding frameworks. Demand-side weaknesses further undermine resilience. On the other hand, fragmented markets, low volumes in key sectors, and limited procurement coordination reduce the commercial viability of European production. Without demand aggregation and reliable market signals, new capacity risks underutilisation.

Finally, the evaluation concludes that **the EU has limited insight into EU and global semiconductor supply chains to support strong crisis preparedness**. Although the ESB substantially improved coordination and early-warning mechanisms were initiated, monitoring should consider a more integrated approach across materials, equipment, design tools, and downstream users. Data collection remains fragmented and sensitive, limiting the ability to anticipate disruptions. Pillar III therefore provides only partial system-level visibility.

Overall, the Chips Act has delivered quickly and credibly on its initial ambition to build European capacity. However, effectiveness in terms of autonomy and resilience depends on whether Europe can now convert infrastructures into industrial output, innovation into scale, and coordination into actionable intelligence.

5.2. Lessons learned

Several lessons emerge from the evaluation regarding the design and implementation of the Chips Act. First, **turning innovation into industrial capacity** requires policy mechanisms that explicitly bridge pilot line infrastructures and manufacturing investments. While the Chips Act successfully created world-class research and validation facilities, experience shows that market-scale production does not emerge automatically from technological capability alone. Future initiatives would benefit from embedding transition mechanisms that facilitate movement from pilot lines into industrial deployment more systematically.

Second, **demand orientation** should be built into industrial policy instruments. The evaluation highlights that supply-side investment alone does not necessarily generate scale or competitiveness in the absence of reliable market uptake. Instruments that support deployment should therefore be accompanied by measures that increase demand, such as procurement coordination or consumption incentives.

Third, **access to finance** must remain central to industrial policy. The evaluation shows that the FOAK framework improved legal certainty for major investments, but certain stakeholders claim that they still face long notifications and State aid procedures, and project-level uncertainty. Late-stage venture capital and institutional investment constraints similarly limit scale-up funding. These factors weaken Europe's competitiveness and slow the growth of globally competitive firms.

Finally, **crisis preparedness depends on high-quality system intelligence**. The evaluation shows that effective monitoring requires up-to-date visibility across the entire value chain, covering not only fabrication, but also materials, packaging, design tools and downstream users. Future frameworks could prioritise improved data collection, shared data infrastructures, and integrated reporting in order to enable timely risk detection and coordinated responses.

ANNEX I – EVALUATION MATRIX

Effectiveness

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
How successful has the EU's intervention been in achieving (or progressing towards) the objectives of the Chips Act? To what extent did the expected changes result from EU action delivered?	What are the outcomes and results of the Chips act on the areas indicated in the objectives? To what extent are these results and impacts resulting from the Chips Act?	Extent to which the intervention's outcomes align with the specific objectives outlined in the Chips Act's intervention logic (e.g., strengthening research leadership, addressing skills shortages, increasing production capacity) The positive or negative effects of the intervention can be linked directly to the interventions of the Chips Act.	Progress against indicators set out in Annex II of the Chips Act Regulation Rate of commitment of Pillar I budget via the Chips JU (JU) Work Programme Number of 'First-of-a-Kind' (FoaK) facilities established and operational Amount of public and private investment mobilised under the Chips Act Number of SMEs and start-ups supported through the Chips Fund Share of stakeholders who report progress towards the objectives (in %) (by MS, type of stakeholder) Contextual information on potential other trends and developments that could explain the observed results	Desk research and document review Targeted online survey, expert interviews, workshops and the OPC Case studies Analysis of results Impact evaluation

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
What has been the quantitative effect of the Chips Act in terms of investment in the European semiconductor industry?	How did the investments levels look like before and after the interventions of the Chips Act? To what extent are the changes in investment levels resulting from the Chips Act?	The volume and type of new of public and private investment mobilised directly attributable to the framework and incentives established by the Chips Act. The positive or negative investments changes can be linked directly to the interventions of the Chips Act.	Total value (€ billion) of public and private investment announced and committed since the introduction of the Chips Act Disaggregation of investment by pillars of the Chips Act, type of facility, value-chain segment, technology nodes and MS Value (€ billion) of State aid approved for FoaK and IPCEI projects R&D expenditures in the EU chips sector since the introduction of the Chips Act, and comparison with non-EU countries Semiconductor patents in the EU since the introduction of the Chips act, compared with non-EU countries FDI inflows into the EU semiconductor sector, attributed to the Chips Act, if possible Comparison of investment trends against the pre-Chips Act baseline Levels of new public and private investments reported by (industry) stakeholders (in EUR) (by Member State, type of investments, policy and pillar focus) Contextual information on potential other trends and developments that could explain investment developments Share of national authorities agreeing that investments occurred due to the Chips Act (in %) (by Member State and policy area) Assessment of the causal link between the EU intervention and the observed changes in investments controlling for potential other factors	Desk research and review of statistics Assessment of costs and benefits, modelling of investment flows attributable to the Act Targeted online survey, expert interviews, workshops and the OPC
Has the Chips Act reduced supply chain dependencies for European industry in practice?	In which areas have supply chain dependencies been reduced and in which areas not? How have the different pillars contributing to reducing supply chain dependencies?	Evidence demonstrates a measurable decrease in reliance on single non-EU sources for critical semiconductor components, materials, or equipment, and an increase in the resilience of EU-based supply chains.	Change in EU's global market share in specific value chain segments (e.g. advanced packaging, SiC/GaN wafers) Analysis of trade data imports/exports of key semiconductor products, linking to relevant pillar efforts Number of new EU-based suppliers for critical materials and equipment, across pillars I and II Perceptions of downstream industrial users (automotive, healthcare, telecoms) on security of supply and how different pillars have impacted this perception Analysis of supply chain mapping exercises conducted under Pillar III	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Desk research on international/ academic evidence Impact evaluation Analysis of results

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
To what extent are the activities and implementation methods suited to protect the EU's security interests and help reinforce the EU's strategic autonomy?	How fitting are the activities and methods of the Chips Act to achieving strategic autonomy and security interests? To what extent has the Chips Act fostered 'managed interdependence' by strengthening partnerships and diversifying supply chain collaborations with non-EU partners?	The governance mechanisms (Pillar III) and investment frameworks (Pillar II) are effectively designed and implemented to anticipate, monitor, and mitigate supply chain disruptions and support production in strategic technology areas. The EU has successfully leveraged the Chips Act to build more resilient supply chains through strategic international cooperation, reducing critical dependencies on single sources while reinforcing its position within a network of reliable global partners.	Contextual information about semiconductor policies and initiatives to increase strategic autonomy and security on other countries, and their evaluation results Number of early warnings issued by the ESB Timeliness of crisis response mechanism activation (simulations or real events) Assessment of the effectiveness of ESB monitoring, warning and crises response Assessment of the functionality and readiness of the Pillar III crisis response toolbox (e.g., priority-rated orders, common purchasing) Analysis of the criteria for FoaK status to assess alignment with strategic technologies Share of stakeholders who state that the ESB is effective (in %) (by Member State, type of stakeholder) Comparative evaluation of the suitability of each pillar's activities and methods in reinforcing strategic autonomy, considering their distinct roles (e.g. R&D, industrial scaling, crisis management) and evidence from other countries Number and value of joint R&D projects or investments with key international partners Analysis of trade data showing diversification of imports for critical semiconductor materials and equipment away from single-country dominance Assessment of the effectiveness of cooperation mechanisms established under international agreements (e.g., EU-US TTC, EU-Japan Digital Partnership) Stakeholder perceptions from EU industry and international partners on the quality and strategic value of the collaboration Evidence of the EU leveraging partnerships to gain access to technologies or markets where it has identified gaps	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Desk research on international/ academic evidence Impact evaluation Analysis of results
In case targets or objectives have not been met or the expected progress has been delayed, what were the causes? Will it be possible to achieve the objectives on time? Were there any mitigating measures taken? What could be alternative targets that may be considered?	Will it be possible to achieve the objectives on time? Were there any mitigating measures taken? What could be alternative targets that may be considered?	Identification of a clear causal link between specific hindering factors (internal or external) and any identified implementation gaps or delays and mitigation measures.	Assessment of progress on each Pillar and activities Variance analysis of actual vs. planned progress against key milestones (e.g. pilot line operational dates) for each pillar Assessment of the causes behind delays and challenges to achieve objectives Analysis of unsuccessful projects and causes of failure Analysis of mitigating actions taken by the Commission/Chips JU Expert and stakeholder opinions on the realism of current targets and potential alternatives, considering the performance and challenges of each pillar Identification of alternative scenarios and targets	Targeted online survey, expert interviews, and workshops State-of-play analysis of global context

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
What external factors have hindered progress towards achieving the objectives of the Chips Act?	What were the challenges or problems the Chips Act faced with its implementation and achieving results? Which of these challenges and problems were due to external factors?	Identification and the impact assessment of specific geopolitical, economic, and technological factors outside the direct control of the EU intervention.	Analysis of competing global subsidy programmes (e.g., US CHIPS Act, China's Big Fund) and their impact on investment decisions Assessment of the impact of global economic conditions (e.g., inflation, energy costs) Analysis of geopolitical events (e.g., trade tensions, export controls) affecting supply chains and their differential impact on each pillar's objectives Identification of unforeseen technological shifts Forecast modelling of EU market share trajectory vs. the 20% Digital Decade target, considering the current pace of each pillar's implementation Identification of causal factors (e.g., administrative delays, funding gaps, market dynamics, geopolitical events) through root cause analysis and process tracing, specifically analysing their impact on each pillar's progress	Targeted online survey, expert interviews, workshops, and the OPC State-of-play analysis of global context Impact evaluation Case studies Policy recommendations analysis
What are the spill-over effects of the Chips Act, if any? How does the Chips Act contribute to horizontal priorities, in particular to Europe's competitiveness and security?	How does the Chips Act contribute to horizontal priorities (e.g., twin transitions and preparedness)? How does the Chips Act contribute to Europe's competitiveness and security?	Evidence of positive or negative unintended effects in adjacent policy areas. Clear contribution to broader EU goals such as the Green Deal, digital sovereignty, and economic security.	Analysis of how Chips Act investments support digitalisation, research and innovation Analysis of how Chips Act investments support the development of energy-efficient semiconductors (Green Deal alignment) Spill-over effects noted by stakeholders (most popular categories of spill-over effects in online survey) Assessment of the Act's role in strengthening the EU's horizontal priorities in green and digital transition Number of patents filed generated from Chips Act-funded research Job creation figures in related sectors (e.g. equipment manufacturing, software development) Case study evidence of technology transfer to other sectors Spill-over effects noted by stakeholders (most popular categories of spill-over effects in online survey) Assessment of the Act's role in strengthening the EU's position in global technology standard-setting bodies	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Analysis of results Case studies

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
Have any concrete benefits for Europe's semiconductor industry and its users materialised?	What are the observed changes in the beneficiary stakeholders' businesses? Are the changes in line with expectations?	Evidence of tangible improvements in competitiveness, innovation, and market access for EU firms and users	Growth in revenue and market share of European semiconductor companies Increased market share of semiconductors produced in the EU in applicable segments Reduction in production downtime for user industries due to chip shortages and the role of Pillars III and II mechanisms specifically Testimonials from companies (beneficiaries and users) on specific benefits gained (e.g. access to pilot lines, improved supply stability, new business opportunities), linking benefits to specific pillars Case study evidence of successful product development or market entry facilitated by the Act, identifying the contributing pillar(s) Comparative analysis of the types and scale of benefits realised across the different pillars	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Case studies Analysis of results and assessment of costs and benefits
To what extent were the technologies selected under the Chips Act relevant, and how well do they lend themselves to industrial technology transfer?	To what extent were the technologies selected relevant to meet changing needs? How well do the technologies led themselves to industrial technology transfer?	The technology focus of Pillar I aligns with future market demand and strategic industrial needs, and clear pathways exist for their adoption by European industry.	Number of industrial partners and research institutions participating in pilot lines Number of licenses and patents resulting from the pilot lines. Expert assessment of the long-term strategic relevance of selected technologies and stages of the semiconductor value chain Analysis of pilot line governance and access models to assess their industry-friendliness Stakeholder feedback on the effectiveness of bridging the "lab-to-fab" gap Assessment of the role of Competence Centres in driving technology transfer Evaluation of the alignment between Pillar I's technological focus and Pillar II's manufacturing investments	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Analysis of results Case studies
How effective have the communication of the Chips Act and Chips Act related activities been?	Did the communication on the Chips Act reach the relevant stakeholders, and across the value chain? What activities were more and less successfully communicated?	Key stakeholder groups are well-informed about the opportunities offered by the Chips Act, and the EU's strategic intent is clearly communicated both internally and globally.	Media monitoring metrics (volume of coverage, engagement metrics, sentiment analysis), for each pillar's specific initiatives where relevant Website and social media analytics for Chips Act-related portals Participation rates at info days and brokerage events Stakeholder awareness levels assessed through surveys, differentiating awareness of each pillar's opportunities Analysis of the clarity and accessibility of communication materials (e.g., call documents, guidance), per each pillar Coverage of Chips Act, assessing the framing and visibility for pillars, if possible	Desk research and document review Targeted online survey, expert interviews, workshops and the OPC Media analysis

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATORS	DATA SOURCES
What is the direct and indirect impact of the Chips Act on the labour market?	What has been the effect on job creation and wages? What has been the effect on skills development and talent attraction?	The intervention has a demonstrable effect on job creation, skills development, and talent attraction within the EU semiconductor ecosystem.	Number of individuals trained through Chips Act-supported initiatives (e.g. Competence Centres, Chips Academies) Number of direct jobs created in new/expanded facilities Wages, employment and skills shortages and vacancies data in the sector (trend data) Data on talent mobility (attraction of researchers/engineers to the EU) Share of stakeholders who report availability of qualified skilled labour (in %) (by MS, type of stakeholder)	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Analysis of results and assessment of costs and benefits Impact assessment
Are the indicators and targets set adequate to measure the success of the Chips Act?	Are the indicators selected suitable for measuring success with semiconductor policy? Are the indicators useful and feasible to monitor and track?	The existing indicators and the overarching Digital Decade target are specific, measurable, achievable, relevant, and time-bound (SMART) for assessing the Act's performance.	Expert review of the relevance and robustness of indicators, including those specific to each pillar Analysis of the methodology and baseline for the 20% Digital Decade target, assessing its suitability as an overarching goal Stakeholder perceptions on the usefulness and adequacy of current monitoring data and framework Comparison with monitoring frameworks of similar initiatives internationally Identification of potential gaps in the current monitoring framework	Targeted online survey, expert interviews, workshops and the OPC Desk research and document review Analysis of results and policy recommendations
How accessible were the activities stemming from the Chips Act and related policies to start-ups and SMEs?	Were SMEs able to apply for and get funding? Were SMEs able to join pilot lines?	Application processes and support structures are designed and implemented in a way that facilitates, rather than hinders, the participation of smaller actors.	Funding from the Chips Act, in particular the Chips Fund, awarded to SMEs and start-ups Number of SMEs and start-ups accessing pilot lines and the design platform Success rates of SME applicants in Chips JU calls compared to large enterprises SME and start-up feedback on the complexity of application procedures and the usefulness of support services (e.g. from Competence Centres) Stakeholder perceptions on the accessibility of activities across the different pillars Case studies of SME or start-up participation Analysis of the design of the Chips Fund to assess its suitability for early-stage companies	Desk research and review of statistics Targeted online survey, expert interviews, workshops and the OPC Case studies Analysis of results

Relevance

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
How well do the original objectives of the Chips Act correspond to current and emerging needs?	What are the current or emerging needs in the European semiconductor ecosystem? What are the original and current objectives of the Chips Act?	The extent to which problems identified in the 2022 Staff Working Document remain pertinent, and the Act's objectives are aligned with new challenges and opportunities that have emerged since its adoption.	Contextual information on recent technological trends (e.g., demand for AI chips) and geopolitical shifts Share of stakeholders who agree that the current strategic focus of the Act is relevant (in %) (by Member State, type of stakeholder) Overlap or mismatch of the original problem definition with the current state-of-play of the semiconductor industry Overlap or mismatch of the objectives of the Act with the strategies of other major semiconductor players (e.g., US, China)	Desk research on market developments and documentary review Targeted online survey, expert interviews, workshops and the OPC Analysis of results
To what extent does the Chips Act address the needs of its main stakeholders?	What are the current or emerging needs and challenges in the European semiconductor ecosystem? How has the Chips Act balanced support between cutting-edge (<5nm) and mature/mainstream semiconductor technologies? Does this balance align with the current and emerging needs of stakeholders?	Key technological, market, and geopolitical developments are identified to determine the current and emerging needs justifying EU intervention. This includes any evolving problems (e.g. new supply bottlenecks, surging demand for AI chips, skills gaps) that have arisen or intensified post-2022. Degree to which the different pillars and instruments of the Chips Act are tailored to the specific needs of key stakeholder groups. The Act's portfolio of support is strategically balanced, addressing both the long-term objective of technological leadership in advanced nodes and the immediate resilience needs of key downstream sectors for mature chips.	Contextual information on needs and challenges: recent industry trends, shock events and data market changes, combined with stakeholder testimonies on needs Share of stakeholders who agree that the Chips Act and the different pillars address their needs/challenges (in %) (by Member State, type of stakeholder) Share of uptake of the different instruments by stakeholder groups (in %) (by Member State, type of stakeholder) Distribution of funding (€ and %) from Pillars I and II allocated to projects targeting cutting-edge vs. mature nodes Number of FoaK facilities approved for advanced vs. mainstream technologies Analysis of demand forecasts from key user industries (e.g., automotive, healthcare) versus the technology focus of supported projects Stakeholder perceptions (industry associations) on the alignment of the Act's focus with their sector's needs Analysis of the criteria for pilot lines and FoaK facilities to assess the weighting given to different technology nodes. Case study evidence on how supported projects address specific supply chain gaps identified by downstream users Difference between reported needs and specific support offered by the Act	Desk research on market developments and documentary review Targeted online survey, expert interviews, workshops and the OPC Analysis of results
To what extent is the Chips Act sufficiently flexible to adapt to emerging needs and changing circumstances?	To what extent has the implementation of the Chips Act responded to relevant political and economic developments?	The Act's implementation mechanisms (e.g., Chips JU work programmes, ESB deliberations) have demonstrated an ability to adjust priorities and actions in response to unforeseen events or	Evidence of the Act's implementation being referenced or adjusted in response to major political statements or economic shock Case studies that demonstrate adaptation (or lack thereof) Share of stakeholders who agree that the strategy is able to adapt and provide testimonies on successful	Desk research and document review Case studies Targeted online survey, expert interviews, workshops and the OPC

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
		new opportunities.	adaptation (in %) (by Member State, type of stakeholder)	
Which parts of the semiconductor value-chain benefit the most from the Chips Act? Which parts of the value-chain are benefiting the least?	Which stakeholders benefit and not from the Act and its pillars? What type of benefits are there and how are they distributed among stakeholders (financial, learning, collaboration, etc)?	The support provided by the Chips Act is distributed across the value chain in a manner that is strategically justified, addressing the most critical gaps without neglecting other important segments.	Breakdown of funding and investment by value chain segment Share of stakeholders that prefer specific parts of the Act (in %) (by Member State, type of stakeholder, part/pillar of the Act) Share of stakeholders that claim that they benefit from specific parts of the Act (in %) (by Member State, type of stakeholder, part/pillar of the Act) Analysis of whether the distribution of benefits and support of the Act aligns with the strategic gaps identified in the problem definition	Targeted survey and mapping and analysis of the state of the value chain Expert interviews, workshops and the OPC Analysis of results
To what extent do the needs/problems addressed by the Chips Act continue to require action at EU level as opposed to intervention at national/regional level?	What are the needs and problems the Chips Act aims to address? What are the needs and problems that national/regional level governance tries to address?	The scale of investment required, the cross-border nature of value chains, and the need for a unified stance in global competition confirm that the rationale for EU-level action remains strong (subsidiarity principle).	Contextual information on the scale of challenges and economies of scale (e.g. global subsidy race) versus the capacity of individual MS to respond Overlap or mismatch between the Act budgets and scope with national semiconductor strategies or other international initiatives Share of stakeholders that claim that an EU-level framework is needed versus purely national initiatives (in %) (by Member State, type of stakeholder)	Desk research and documentary review of semiconductor policies in Europe Analysis of policy options considering international dimensions Targeted online survey, expert interviews, workshops and the OPC

Efficiency

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
How operationally efficient is the Chips for Europe Initiative?	How efficient was the implementation of the Chips for Europe Initiative? How efficient is the application process for initiatives sourcing funds from different streams?	The resources (financial, human, administrative) utilised by the Chips for Europe Initiative are proportionate to the outputs and results achieved. Application and funding processes are streamlined and minimise administrative burden.	Administrative costs as a percentage of the total budget Average time-to-grant and time-to-pay for Chips JU projects Cost-benefit analysis of key actions (e.g., pilot lines) Beneficiary and applicant feedback on the complexity and burden of application procedures and multi-stream funding applications Analysis of processes for projects combining funds (e.g., from HE and Digital Europe) to identify bottlenecks	Cost-benefit analysis Desk research: Chips JU financial reports and internal control documents, European Court of Auditors' reports Stakeholder consultations: survey of applicants and beneficiaries, interviews with Chips JU staff and with beneficiaries who applied for (multi-stream) funding
Is the governance structure of the Chips JU sufficiently agile to implement the objectives of the Chips Act and adapt to technology and market developments?	Do the decision-making processes, roles, and interactions within the Chips JU's governing bodies enable it to respond swiftly to new market and technology developments?	The implementing bodies possess the necessary human resources, technical expertise, and administrative capacity to effectively manage their respective tasks under the Chips Act.	Assessment of decision-making processes of the Chips JU's governing bodies Assessment of the roles and interaction between the Public Authorities Board, the Industrial and Research Board, and the Executive Director Analysis of the time taken to launch new calls or adapt work programmes in response to identified needs, market or technology shifts Stakeholder perceptions of the JU's agility and responsiveness Comparison with governance models of similar international initiatives	Desk research: Chips JU founding regulation and rules of procedure; minutes of Governing Board and Public Authorities Board meetings Targeted interviews: with Chips JU management, board members, and parent DGs (CNECT, RTD), interviews with industry representatives Formulation and analysis of policy recommendations
How well-equipped are the relevant implementing bodies such as the Chips JU, the European Commission, the EIB, the EIF, and the EIC to implement the Chips Act?	Do the Chips JU, Commission, EIB, EIF, and EIC possess the necessary resources to effectively coordinate?	The implementing bodies possess the necessary human resources, technical expertise, and administrative capacity to effectively manage their respective tasks under the Chips Act.	Staffing levels and expertise profiles within each body relative to their mandated tasks Analysis of budget execution rates for administrative expenditure Self-assessment by the bodies of their capacity and identification of any resource gaps Analysis of coordination mechanisms between the different implementing bodies Stakeholder feedback on the professionalism and expertise of the bodies	Desk research: annual reports and management plans of the Chips JU, EIB, EIF, EIC, other reports as applicable Targeted interviews and surveys: with management and operational staff from all named implementing bodies
How efficient is the State aid approval process for First of a Kind (FoaK) facilities and IPCEI projects?	Are the duration, complexity, and administrative burden of the State aid notification and approval process for FoaK and IPCEI	The duration and complexity of the State aid notification and approval process are proportionate and do not create undue delays that jeopardise	Average time from pre-notification to final Commission decision for FoaK and IPCEI projects in the semiconductor sector Comparison with State aid approval times in other sectors Feedback from MS and companies on the clarity of	Desk research: analysis of public State aid decisions and timelines Targeted interviews: with officials from DG COMP, DG CNECT, relevant Member State ministries, and companies that have undergone the

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
	projects appropriate and timely?	strategic investments	guidance and the administrative burden of the process Analysis of the interaction between the Commission (DG COMP, DG CNECT) and notifying parties Comparison with processes in other sectors	process
How complementary has the IPCEI on Microelectronics and Communication Technologies (9) been to the Chips for Europe Initiative to achieve the objectives of the Chips Act?	Do the two instruments operate in a complementary manner, avoiding overlaps and featuring sufficient coordination to form a coherent support landscape?	Extent to which the IPCEI and the Chips for Europe Initiative operate in a synergistic manner, targeting different but complementary aspects of the R&D&I chain, avoiding overlaps and reinforcing mutual objectives	Mapping of projects funded under both instruments to identify areas of focus and potential overlap or synergy Analysis of coordination mechanisms between the Commission services managing the IPCEI and the Chips JU Stakeholder views on how the two instruments interact and whether they form a coherent support landscape	Desk research: IPCEI project documentation; Chips JU work programmes and funded project lists Targeted interviews: with Commission officials (DG COMP, DG CNECT), Chips JU staff, and beneficiaries of both instruments State-of-play analysis: to map the broader policy landscape.
What is the extent of the administrative and financial burden on beneficiaries of the Chips Act?	What are the quantifiable administrative and financial costs for beneficiaries, and are the reporting and auditing requirements perceived as clear and streamlined?	The reporting, auditing, and administrative requirements for beneficiaries are streamlined, clear, and proportionate to the funding received	Estimation of person-hours and financial costs incurred by beneficiaries for administrative compliance (reporting, audits) e.g. using the Standard Cost Model Number of reporting requirements and frequency. Beneficiary survey responses on the perceived level of administrative burden Stakeholder perceptions on specific burdens and pain points of beneficiaries Identification of specific sources of burden (e.g., complex financial reporting, duplicative information requests) and their relative weight	Desk research: analysis of reporting and auditing requirements and comparison with the administrative burden of other EU programmes Cost-benefit analysis: specific component on administrative burden Stakeholder consultations: survey of beneficiaries with dedicated questions on administrative burden; workshop and interviews to discuss specific pain points
Have any inefficiencies in the implementation of the Chips Act been identified? Could the implementation of any of its components be done in a more efficient way? What potential simplification and cost-reduction measures should be considered?	What specific bottlenecks, redundancies, or overly complex procedures exist, and what concrete, feasible simplification measures can be proposed to address them? Where can the implementation of the Chips Act be simplified and made more efficient?	The evaluation identifies specific bottlenecks, redundancies, or overly complex procedures in the Act's implementation and proposes concrete, feasible measures for simplification.	Mapping and analysis of implementation processes and a catalogue of potential simplification measures (e.g. streamlining application forms, harmonising reporting across programmes, greater use of lump sums). Stakeholder validation of proposed measures Cost-benefit assessment of proposed simplification measures	Synthesis of findings from all other evaluation questions Stakeholder consultations: dedicated questions in surveys and interviews on simplification ideas, workshop discussion Cost-benefit analysis: analysis of unjustified cost elements Policy recommendations analysis: formulation and analysis of simplification options
How efficient is the overall governance of the Chips Act?	Are the roles and responsibilities between the Commission, ESB, and Chips JU clearly defined and are the information flows and decision-making processes between them efficient?	The governance structure, including the roles of the Commission, the ESB, and the Chips JU, ensures coherent, timely, and cost-effective implementation of the Act as a whole.	Analysis of the clarity of roles and responsibilities between the different governance bodies Assessment of the efficiency of information flows and decision-making processes between the ESB, Commission, and Chips JU Identification of any governance gaps or overlaps Stakeholder perceptions of the overall governance efficiency	Desk research: analysis of the Chips Act Regulation and internal working arrangements between the bodies Targeted interviews: with members of all key governance bodies (Commission, ESB, Chips JU)

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
Have the skills and talent initiatives under the Chips Act been efficient in addressing sector needs?	Do the resources invested in talent development, attraction, and retention yield a measurable increase in qualified professionals who meet the industry's skills needs?	The resources invested in skills initiatives have yielded a measurable increase in the availability of qualified talent, addressing critical skills gaps identified by the industry.	Ratio of programme graduates who secure employment in the EU semiconductor sector within a set timeframe Metrics on the international recruitment of top-tier talent into EU-based companies and research institutions Analysis of the administrative efficiency of establishing and running skills academies and competence centres Employer or association feedback on the quality and relevance of skills provided by the new training programmes Testimonials on the attractiveness of the EU as a destination for a career in semiconductors	Desk research: analysis of programme budgets and enrolment data from Chips Academies and competence centres; reports from the European Chips Skills Academy (ECSA Stakeholder consultations: surveys and interviews with the semiconductor industry, heads of training institutions Cost-Benefit Analysis: to assess the cost-effectiveness of skills initiatives.

Coherence

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
To what extent is the Chips Act coherent with other EU, national and regional interventions that have similar objectives? To what extent have synergies been achieved? What could be done to improve the coherence with other related EU, national or regional initiatives?	To what extent have synergies been achieved with other related initiatives? What could be done to improve coherence with other EU, national, or regional initiatives?	Extent to which the Chips Act complements and reinforces other relevant policies without creating contradictions or duplications. Existence of mechanisms in place to foster synergies.	Evidence of joint planning, coordination mechanisms, or mutual reinforcement between the Chips Act and other initiatives Identification of any instances of policy conflict, redundancy or of synergies and cooperation between the Chips Act and other EU policies, including the framework programmes, the Single Market, competition policy. Stakeholder perceptions on the coherence of the overall policy landscape.	Desk research: analysis of HE, RRF plans, and IPCEI documentation or other relevant documentation at national and regional level Interviews: with MS officials, regional authorities, and managers of national programme
To what extent the various components of the Chips Act generated synergies and/or compensated possible trades-offs among them?	How do the three pillars of the Chips Act interact to create a mutually supportive framework? How are potential trade-offs identified and managed?	Extent to which the three pillars of the Chips Act are implemented in a mutually supportive way in terms of internal coherence.	Analysis of the functional links between the three pillars Evidence of information sharing and joint decision-making between the bodies responsible for each pillar Identification of any trade-offs (e.g., focus on cutting-edge in Pillar I vs. need for mature nodes in user industries) and how they are managed	Desk research: analysis of the Chips Act Regulation, the overall intervention logic and implementation documents Targeted interviews, surveys and workshop: with officials from the Commission, Chips JU, and ESB, focusing on inter-pillar coordination
To what extent is the Chips Act coherent with actions funded under EU Programmes listed in Annex III of the Chips Act Regulation, the Recovery and the Resilience Facility, the Digital Decade Policy Programme objectives and targets (10) and other EU programmes with similar objectives? Have synergies materialised with EU Programmes listed in Annex III of the Chips Act Regulation? In which areas should synergies be fostered?	Have synergies materialised with the EU Programmes listed in Annex III of the Chips Act Regulation? In which areas should synergies be fostered?	The extent to which the Chips Act is implemented in alignment with the objectives and funding streams of related EU programmes, leveraging them for mutual benefit and avoiding fragmentation of effort.	Detailed mapping of the links and potential synergies between the Chips Act and other funding programmes (HE, Digital Europe, RRF, etc.) Analysis of the alignment of Chips Act objectives with the Digital Decade targets Review of Member State RRF plans and its use for coherence with Chips Act goals Evidence of concrete synergies that have materialised Stakeholder suggestions on areas for future synergies	Desk research: analysis of selected EU programmes Targeted interviews and workshops with officials from relevant Commission DGs (e.g., EMPL, REGIO, ECFIN)
To what extent is the Chips Act coherent with current wider EU policies and priorities?	How does the Chips Act contribute to the European Green Deal and the digital transition?	Extent to which the Chips Act supports and is supported by major EU strategic priorities, such as the European Green Deal, the digital transition, open strategic autonomy, and economic security.	Analysis of how Chips Act contributes to key EU policy objectives Assessment of the Act's role in the broader digital, green and competitiveness agenda Review of Commission policy documents and communications to assess the integration of the Chips	Desk research: Analysis of key Commission Communications and Strategies on the Green Deal, Digital Decade, and Economic Security etc. as well as other documents and communications, analysis of

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
	How does the Act support the EU's goals for open strategic autonomy and economic security?		Act into the broader policy framework Review of selected commentaries and policy papers published on the Chips Act	European Council conclusions and European Parliament resolutions Policy recommendations analysis: this task will explicitly consider coherence with wider EU priorities
How coherent is the governance architecture of semiconductor policy in Europe? In particular, how do the different layers of governance and coordination interact with each other? How do they ensure a coherent approach towards industrial and institutional stakeholders?	How do the different layers of governance and coordination (e.g., Commission, ESB, Chips JU) interact with each other? How do they ensure a coherent approach towards industrial and institutional stakeholders?	Extent to which the different governance bodies interact effectively, with clear communication channels and a shared strategic direction, presenting a unified front to stakeholders.	Mapping of the governance architecture and the formal/informal links between its components Perceptions of representatives from various levels of governance Expert feedback on the clarity and coherence of their interactions with the governance system Identification of any coordination failures or jurisdictional ambiguities	Desk research: analysis of governance documents for all relevant bodies Targeted interviews, workshops: with experts and representatives from all layers of the governance architecture and with stakeholders who interact with them (e.g., industry associations).

EU added value

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
Which benefits were achieved so far that go beyond what Member States could achieve while acting alone? Which concrete benefits does the Chips Act offer that go beyond other existing national or regional initiatives with similar objectives?	Which concrete benefits does the Chips act offer that go beyond the benefits of other existing national or regional initiatives with similar objectives?	Extent to which the Chips Act has generated outcomes of a scale, scope, or nature that would not have been feasible through uncoordinated national or regional actions.	Evidence of large-scale, cross-border collaboration (e.g., pan-EU pilot lines) that would be difficult to organise nationally Stakeholders agree that their MS could not implement changes without TSI support (in %) (by Member State) Identification of benefits related to critical mass, coordination, and a unified EU approach Analysis of the EU's increased leverage in international partnerships and trade negotiations due to a unified strategy Assessment of the creation of a more coherent and attractive single market for semiconductor investment, reducing fragmentation	Desk research: comparison of the achievements of the Chips Act with the scale and scope of purely national semiconductor initiatives Case studies: cases evidencing the EU added value of cross-border projects. Targeted interviews: with MS and industry on the benefits of EU-level coordination. Impact evaluation: to quantify the 'EU effect' against a baseline of uncoordinated national actions.
To what extent does the Chips Act promote cooperation among Member States to achieve its objectives?	How has the European Semiconductor Board (ESB) functioned as a forum for Member State cooperation? Has the Chips Act framework led to joint strategic planning or coordinated national investments?	Extent to which the Act has demonstrably incentivised and facilitated collaboration, information sharing, and joint investment among MS in the semiconductor field.	Number of MS participating in Chips JU projects Volume of cross-border investment within the EU semiconductor sector Analysis of the functioning of the ESB as a forum for MS cooperation and information exchange Evidence of joint strategic planning or coordinated national investments fostered by the Chips Act framework Stakeholder perceptions of the level and quality of inter-state cooperation	Desk research: analysis of the composition of project consortia in Chips JU calls; ESB meeting minutes and other relevant documents Targeted interviews and workshops: With Member State representatives on the ESB and participants in cross-border projects.

Recommendations and follow-up questions

EVALUATION QUESTION	SUB-QUESTION	JUDGEMENT CRITERIA	INDICATOR	DATA SOURCES
What are the key shortcomings or constraints of the Chips Act in fulfilling its stated aims?	What are the main weaknesses in the design of the Chips Act (e.g., funding levels, scope, governance structure, monitoring framework)? What are the most significant bottlenecks and challenges in the implementation of the Act (e.g., administrative burden, state aid)?	Identification of the main weaknesses and challenges in the design and implementation of the Chips Act.	Synthesis of the findings from the evaluation of the five main criteria (effectiveness, efficiency, relevance, coherence, EU added value) to identify key shortcomings Stakeholder identification of the main constraints they face. Stakeholder identification of the main constraints they face.	All data sources used for the evaluation Specific questions in stakeholder consultations on shortcomings and constraints
What key lessons and actionable recommendations can be drawn for the future of EU semiconductor policy?	Which mechanisms and instruments of the Chips Act have proven most successful and should be reinforced in future policies? What specific, evidence-based recommendations can be made to improve the design, governance, and implementation of EU semiconductor policy? How can future policy be designed to be more flexible and adaptive to the highly dynamic technological and geopolitical landscape?	Formulation of evidence-based and actionable recommendations for improving EU semiconductor policy	Synthesis of the findings from the evaluation of the five main criteria (effectiveness, efficiency, relevance, coherence, EU added value) to identify key shortcomings Stakeholder identification of the main constraints they face. Stakeholder identification of the main constraints they face.	All data sources used for the evaluation Specific questions in stakeholder consultations on shortcomings and constraints

ANNEX II – MAIN POINTS OF COMPARISON

The main points of comparison are:

- The situation before the intervention (2021);
- The situation during the evaluation of the Chips Act (using monitoring data, evaluation and impact assessment findings, 2025).

It must be noted that some initiatives mentioned below were expected to be rolled out later compared to others, which explains why some elements have progressed less two years after entry into force of the Chips Act.

Table 2. Main points of comparison

Point of comparison	Value before the Chips act	Value at the time of the evaluation
EU global market share ([112])	2021: 8.9%	2025: 10.5%
Investment mobilised (FoaK State aid cases)	2021: n.a.	2025: EUR 32 billion
The number of beneficiaries involved in the actions supported by the Initiative	2021: n.a.	2025: 514
The number of unique legal entities involved in the actions supported by the Initiative	2021: n.a.	2025: 313
The number of design tools developed or integrated under the Initiative	2021: n.a.	2025: 0
The total amount co-invested by the private sector in design capacities and pilot lines under the Initiative	2021: n.a.	2025: 0
The number of users of semiconductors or user communities seeking, and the number of users of semiconductors or user communities obtaining, access to design capacities and pilot lines under the Initiative	2021: 0	2025: Up to 60 SMEs/start-ups using pilot lines
The number of businesses, which have used the services of national competence centres supported by the Initiative	2021: 0	2025: 20
The number of persons who have successfully concluded training programmes supported by the Initiative to acquire advanced skills and training on semiconductor technologies and quantum technologies	2021: 0	2025: 100 (via competence centres)
The number of active competence centres in the Union in the context of the Initiative	2021: 0	2025: 30
The number of start-ups, scale-ups and SMEs that have received venture capital from the Chips Fund activities and the total amount of capital investments made.	2021: 0	2025: 55 companies (EUR 354 million equity investment and EUR 62 million in grants)
The amount of investment by companies operating in the Union,	2021: 0	2025: tbd

([112]) Source: Contract CNECT/2022/MVP/0084, *Semiconductors market data by feature size, sector and region*, IDC, September 2025

Point of comparison	Value before the Chips act	Value at the time of the evaluation
including by segment of the value chain in which they operate.		
Number of working pilot lines	2021: 0	2025: 5
Number of training programmes launched	2021: 0	4 (through competence centres)
Number of SMEs/start-ups receiving funding	2021: 0	Chips Fund: 55 startups/SMEs
Number of FoaK State aid projects supported	2021: 0	2025: 11
Number of semiconductors IPCEI projects	2021: 0	2025: 68
ESB operational	2021: No	2025: Yes
Emergency toolbox operational	2021: No	2025: Partly
SCAN system operational	2021: No	2025: Yes

ANNEX III – OVERVIEW OF BENEFITS AND COSTS

Costs of the European Chips Act

The European Chips Act represents a significant financial commitment by the EU institutions and EU Member States to strengthen the semiconductor ecosystem. It generates direct financial and administrative costs as well as indirect costs across its three pillars.

Direct Financial Costs

Direct financial costs cover public expenditure and capital investments required to implement the Act, borne mainly by EU and national administrations, with complementary private investment.

Pillar I

Pillar I entails large public financial commitment, channelled through grants, Joint Undertaking contributions, and equity-type instruments. Citizens and consumers do not face direct financial costs, as funding comes from EU and national budgets. At EU level, as of November 2025, total public expenditure under Pillar I is around EUR 1,960.5 million: EUR 1,831.2 million for pilot lines, EUR 92.3 million for competence centres, EUR 25 million for the Design Platform, and EUR 12 million for design-related activities. The amount for pilot lines includes capital investment and operational expenditure, combining Horizon Europe and Digital Europe resources. The EU has foreseen about EUR 120 million over four years to competence centres, which – with EUR 92.3 million – is expected to be slightly lower in commitments due to Iceland not opting for a competence centre and several countries not going for the maximum amount of EUR 4 million over 4 years. To establish and operate the Quantum Chip pilots and the Design Platform, amounts of around EUR 200 million and EUR 400 million respectively are foreseen. Six Framework Partnership Agreements have been signed for quantum chip pilots. These come without financial commitment. First commitments for quantum chip pilots are expected for beginning of 2026. EUR 37 million has been committed on the Design Platform and design-related activities. The Chips Fund adds EUR 425 million: EUR 300 million via the EIC Accelerator, which has awarded EUR 62 million in grants and EUR 238 million in recommended equity investment to 24 startups through the dedicated Semiconductor and Quantum Technologies challenge and EUR 125 million via InvestEU, where EUR 68 million has been signed or approved with four financial partners, resulting in EUR 116 million in equity investment to 31 companies.

At national level, public expenditure stands at roughly EUR 1,957.3 million, including EUR 1,862.1 million for pilot lines and EUR 95.3 million for competence centres, with national support broadly matching EU contributions. No national financial costs were incurred for the Design Platform so far. Businesses do not yet face formal direct financial charges under the grant schemes so far. However, access to pilot lines, design platform, and quantum chip pilots, as well as support from competence centres come with a cost.

Pillar II

Pillar II focuses on security of supply and resilience through large-scale manufacturing facilities, potentially supported by State aid. Citizens and consumers do not bear direct financial costs, which fall instead on national administrations granting State aid and on private investors financing new fabrication plants. Eleven State aid decisions for FOAK facilities

represent a total public–private investment of EUR 32.2 billion. Total investments for some State aid supported projects are not disclosed. In parallel, the IPCEI on microelectronics and communication technologies covering research and innovation projects mobilises EUR 21.8 billion, of which EUR 13.7 billion is private investment and EUR 8.1 billion is State aid. For firms, the main direct financial costs are the capital expenditure for constructing and equipping fabs and the recurring operating costs (labour, utilities, maintenance), although detailed operating cost data are not yet available. No additional direct EU-level financial cost is recorded, as public investments are made by Member States, and the EU role is largely regulatory and supervisory.

Pillar III

Pillar III establishes monitoring and crisis response mechanisms, with modest direct financial implications. Citizens and consumers do not incur direct costs. For businesses, potential financial impacts arise only if crisis-stage measures are activated. Priority-rated orders could force manufacturers to prioritise certain customers, generating opportunity costs in the form of foregone revenues, disruptions, and strained commercial relationships. Export restrictions and information obligations would add compliance costs for semiconductor producers and downstream exporters. However, no crisis stage has been declared, and no such costs have materialised. For administrations, crisis coordination and enforcement costs remain minimal at this stage, although EU and national authorities would face higher resource demands if the crisis toolbox were used.

Direct Administrative Costs

Direct administrative costs comprise the human resources and operational effort required to manage, administer, and monitor the Act's instruments, for both participating firms and public authorities.

Pillar I

Administrative costs in Pillar I stem from managing multiple funding instruments and the associated application, due diligence, contracting, and monitoring processes. Citizens and consumers incur no administrative costs. For businesses, the administrative burden is perhaps most visible for SMEs and start-ups applying to the Chips Fund. A standard cost model suggests an average of 70 person-days (560 hours) per beneficiary for applications, due diligence, and reporting, at EUR 50-60 per hour, yielding about EUR 1.7 million in total for the 55 projects, or roughly EUR 30,000 per project. This number only considers selected proposals. Proposals that are not selected also make considerable investments to apply.

Across all Pillar I grants, an estimated 10-20 person-days per application (midpoint 15 days or 120 hours) at EUR 50 per hour for 514 participants in 44 projects results in around EUR 3 million in administrative and compliance costs, equivalent to about EUR 0.75 million per year over four years.

At EU level, managing the Chips Fund costs around EUR 5.6 million, assuming 160 person-days per funded project at EUR 80 per hour, or roughly EUR 100,000 per project. Administrative costs for other Pillar I instruments can be deducted from annual budgets of the Chips JU. Salary costs increased from EUR 3.9 million in 2023, before the Chips Act entered into force, to EUR 7.0 million in 2025. National administrations incur about EUR 0.7 million

(EUR 0.2 million per year) in administrative costs, based on roughly 25 person-days per project across relevant ministries and agencies.

Pillar II

Pillar II administrative costs relate to the State aid lifecycle. Citizens and consumers do not bear these costs. For businesses, subsidised firms are estimated to spend about 50 person-days per year (400 hours) on State aid applications, audit files, and reporting, at around EUR 80 per hour. This corresponds to approximately EUR 32,000 per beneficiary per year, or about EUR 1.0 million annually for a stylised set of 30 subsidised projects. At EU level, about 40 person-days per project per year (320 hours) at EUR 90 per hour imply around EUR 28,800 per project, or EUR 0.9 million per year across 30 projects. Nationally, preparing and notifying aid, liaising with the Commission, issuing decisions, and checking compliance is estimated at 60 person-days per project per year (480 hours) at EUR 80 per hour, i.e. EUR 38,400 per project per year or about EUR 1.2 million annually for 30 projects.

Pillar III

The administrative costs of Pillar III arise from the supply chain monitoring mechanism and crisis coordination structures. Citizens and consumers do not incur these costs. For businesses, regular monitoring surveys impose a recurring burden: if around 50 key semiconductor firms each spend roughly 160 hours (20 person-days) per year compiling and reporting data at EUR 70 per hour, the total annual compliance cost is about EUR 0.6 million, or EUR 11,000-12,000 per firm. Additional costs from consultations and crisis protocols would emerge only if these tools were used; to date, they remain minimally deployed.

At EU and national level, monitoring requires around eight full-time equivalents across DG CNECT and the ESB at roughly EUR 120,000 per FTE, plus around EUR 0.5 million in analytical support contracts, bringing annual EU monitoring costs to about EUR 1.5 million. For national administrations, assuming in each of the 27 Member States about 0.5 FTE (≈800 hours a year) in relevant ministries and agencies is devoted to data provision at EUR 70/hour, the annual national administrative cost of feeding the EU monitoring mechanism is roughly EUR 1.5 million in total, or about EUR 55 000 per Member State.

For national administrations, crisis coordination and legal enforcement costs involving competition, customs, and trade authorities would increase if measures were activated, but they remain negligible in the absence of a declared crisis.

Indirect Costs

Indirect costs reflect potential distortions, opportunity costs, and unintended effects that are harder to quantify but relevant for overall efficiency.

Pillar I

Under Pillar I, citizens and consumers do not directly bear indirect costs. For businesses, there is a risk of market distortion and crowding out: non-beneficiary firms may face competitive disadvantages, and private investors may be displaced as public funding shapes investment patterns. Resource misallocation is possible if sizable public support diverts efforts from more productive alternatives. Universities and research and technology organisations may also face overlapping mandates and redundancy with other projects. At EU level, multiple funding

streams (Horizon Europe, Digital Europe, joint procurement) risk inefficient budget allocation if coordination is insufficient. National governments face similar risks of duplication if responsibilities between national and EU initiatives are not clearly aligned.

Pillar II

Given the scale of manufacturing support, Pillar II indirect costs are potentially more significant. For citizens and local communities, major fabs entail high water, energy, and land consumption, which can stress local infrastructure and the environment. For firms, opportunity costs arise because large-scale State aid for fabs may limit resources available for SMEs and early-stage R&D, potentially crowding out innovation-focused support. Facility operators face substantial environmental compliance costs, while local and regional authorities may need to upgrade infrastructure and, in some cases, subsidise utilities. For national administrations, devoting sizeable budgets to semiconductor manufacturing implies trade-offs with other priorities such as SMEs, research, or social policy. If crisis-related export restrictions and information obligations were activated, they could provoke retaliatory action by trading partners and disrupt exports from downstream industries, causing further indirect losses.

Pillar III

Indirect costs under Pillar III are largely contingent. Citizens and consumers could be affected if export controls triggered retaliatory measures that influence prices or availability of goods. For businesses, crisis measures such as export controls and priority-rated orders could restrict market access and disrupt commercial relationships, creating opportunity costs beyond direct compliance. To date, no crisis stage has been declared, so these costs remain hypothetical; they would materialise only if the crisis response toolbox were deployed.

Benefits of the European Chips Act

The Act is designed to generate substantial benefits along the semiconductor value chain, from R&I infrastructure to manufacturing capacity and more resilient supply chains. These benefits can be grouped into direct (immediate outputs and outcomes) and indirect (longer-term systemic effects).

Direct Benefits

Direct benefits include infrastructure established, investment leveraged, jobs created, and enhanced monitoring and coordination capabilities.

Pillar I

Pillar I directly builds technology infrastructures and supports SMEs and start-ups. Quantitatively, five advanced pilot lines are operational in 2025, providing cutting-edge fabrication and packaging capabilities to European firms. Around 60 SMEs and start-ups are already using these facilities, with individual lines expecting dozens of SMEs per year, multiple prototypes, and multi-project wafer runs. A network of 30 competence centres across Member States and Norway supports skills development and technology diffusion; early evidence shows centres training engineers and supporting SMEs, indicating practical uptake.

The Design Platform, currently being established, will provide shared design infrastructure through dedicated coordination, design enablement teams, and cloud-based tools.

The Chips Fund has backed 55 projects with EUR 62 million in grants and EUR 354 million in equity, offering risk capital to innovative firms. A leverage ratio of about 5 suggests each euro of funding mobilises roughly EUR 5 from national and participant investment. The Chips Fund's EUR 425 million EU contribution is expected to crowd in more than EUR 2 billion in additional private and EIF resources. For EU and national administrations, the establishment of a coordinated European semiconductor research ecosystem and strong leverage of national and private funds are key direct benefits.

Pillar II

Pillar II directly increases European manufacturing capacity, mobilises substantial private investment and generates high-quality employment. Semiconductor manufacturers and downstream industries gain new EU-based capacity from eleven FOAK facilities with total investment of EUR 32.2 billion, improving access to local production and reducing exposure to external bottlenecks. Companies benefit from an estimated 16 000 direct high-skill fab jobs and roughly 30 000 indirect jobs in suppliers and services once the FOAK pipeline is fully built out, with a direct wage bill in the order of EUR 0.9 billion per year that supports regional incomes, tax bases and local supply chains. Given total FOAK investment of EUR 32.2 billion and typical aid intensities in the 30-50% range, firms are likely contributing roughly EUR 16-22 billion of private co-investment, corresponding to about 1-1.5 EUR of private funding for every Euro of public support. Overall semiconductor investment commitments in Europe now exceed EUR 80 billion ([113]), and demonstrate a strong multiplier effect of State aid. Technological upgrading through smaller technology nodes, advanced packaging technologies and wide-bandgap power electronics strengthens the capabilities of EU semiconductor firms, gives downstream industries access to advanced chips produced in Europe, and supports long-term competitiveness and sovereignty in critical semiconductor value chains, thereby reinforcing the industrial base of the EU and its Member States.

Pillar III

Pillar III directly improves supply chain visibility and coordination. While citizens and consumers are not explicit primary beneficiaries, better intelligence on supply-demand conditions can help avoid or mitigate disruptions, supporting market stability. For businesses, the monitoring mechanism improves predictability and reduces uncertainty by providing information on demand trends and supply bottlenecks across the value chain, leading to better planning and investment decisions. For EU and national administrations, the monitoring system and European Semiconductor Board provide a stronger evidence base for policymaking, enable earlier identification of risks, and support more timely, targeted use of crisis instruments if needed.

([113]) This figure represents both announced and planned investments in the context of Pillar II FOAK projects and past microelectronics IPCEIs.

Indirect Benefits

Indirect benefits are the broader, longer-term effects on innovation, resilience, skills, and competitiveness that build on the Act's direct outputs.

Pillar I

Pillar I indirectly reinforces the innovation ecosystem, human capital, and downstream sector performance. Citizens and consumers benefit from a more innovative economy and stronger EU industrial competitiveness in sectors such as automotive, artificial intelligence, and defence, which depend on advanced semiconductors. Students, engineers, and technicians gain from expanded training opportunities and better employment prospects. For businesses, innovation and knowledge spillovers emerge as more firms access pilot lines and competence centres: about 60 SMEs and start-ups already use pilot lines, with around 41% of supported entities being newcomers, showing that the initiative opens up the ecosystem. At least 100 trainees across several programmes demonstrate early progress in skills development. SMEs and start-ups benefit from technology diffusion and collaboration, while larger firms gain from supply chain synergies and access to innovations coming out of publicly supported infrastructure. Upcoming talent development calls of EUR 45 million in 2026 are set to deepen these effects. Downstream sectors gain through more dependable chip supply and productivity improvements. For EU and national administrations, enhanced resilience and reduced dependency on external fabrication capacity, combined with a more skilled workforce, constitute important strategic benefits, with each Member State hosting at least one competence centre and early evidence of local spillovers.

Pillar II

Pillar II indirectly improves supply chain resilience, fosters regional development, and raises global competitiveness. For citizens and consumers, the existence of critical semiconductor capacity within Europe reduces vulnerability to external shocks, while communities near manufacturing clusters benefit from increased economic activity and a more dynamic innovation environment. Regional clustering in locations such as Dresden and Crolles generates multiplier effects as suppliers, services, and skilled workers concentrate around anchor fabs. For businesses, more resilient EU supply chains translate into reduced exposure to global disruptions, while knowledge transfer and spillovers strengthen the wider innovation system through collaborations between fabs, equipment providers, and research institutes. Increased global competitiveness allows EU semiconductor firms to remain at or near the technological frontier rather than relying on foreign competitors, offering strategic advantages. For public authorities, stronger supply chain security and reduced strategic vulnerability demonstrate the value of coordinated industrial policy and provide a template for future initiatives in other critical sectors.

Pillar III

Pillar III indirectly supports better market functioning, more responsive policy, and long-term optimisation of semiconductor supply chains. Citizens and consumers benefit from more stable markets and improved supply continuity, supported by the existence of crisis-response structures even if they are not yet activated. For businesses, systematic data collection and analysis can dampen extreme inventory cycles and help align capacity with demand, reducing costly mismatches. For EU and national administrations, the information and analytical

capabilities developed under Pillar III enable more evidence-based decisions, both in crisis situations and in routine adjustments to the policy framework governing the semiconductor sector.

CBA tables by pillar

Table 3. Pillar I CBA table

	Overview of costs and benefits identified in the evaluation: Pillar I							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
Direct financial costs	**Public expenditure/grants funding**	Recurring (annual)	No financial costs incurred.		No financial costs incurred		**EU: total of EUR 1960.5 million** (92.3 million for Competence Centres, 25 million for Design Platform, 1831.2 million for Pilot lines, and 12 million for design-related activities). **National: total of EUR 1957.3 million** (95.3 million for Competence Centres, and 1862.1 million for Pilot lines).	
	Capital investment and operational expenditure to Pilot lines	One-off + Recurring (annual)	No financial costs incurred.		Industry consortia and RTOs cost-sharing, in-kind contributions, cost-sharing for pilot line operations cannot be reliably isolated.		**EU: total of EUR 1831.2 million** (898.5 million for HE grants, 45.1 million for DEP grants, and 887.7 million for DEP JPA). **National: total of EUR 1862.1 million** (554.3 million for HE grants, 45.1 million for DEP grants, and 1262.8 million for DEP JPA).	
	Capital investment and operational expenditure to competence centres	One-off + Recurring (annual)	No financial costs incurred.		No financial costs incurred. Full network-wide numbers regarding operational expenditure are not available yet. Illustrative data show that competence centre RO-SMARTYS trained 50 engineers and supported 20 SMEs, while LMCC hired 28 staff.		**EU: total of EUR 92.3 million for 4 years** (1 million per year per competence centre, 27 MS + Norway, and a support action). **National:** total of **EUR 95.3 million for 4 years** (1 million per year per competence centre, 27 MS + Norway).	
	Capital investment and operational expenditure to Design Platform	One-off + Recurring	No financial costs incurred.		No financial costs incurred.		**EU: total of EUR 265 million** (the 2024 Call for Expression of Interest and a EUR 25 million Coordination and Support Action in order to select a central consortium, referred to as the PCT, and three 2025 calls: EUR 5 million call for Coordination and Support Actions to set up and integrate Design	

	Overview of costs and benefits identified in the evaluation: Pillar I							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
							Enablement Teams, EUR 15 million call for tenders for the central cloud infrastructure that will support the operation of the Design Platform, and EUR 220 million Grant to identified beneficiary) **National: no financial costs incurred.**	
	Chips Fund support	Recurring	No financial costs incurred.		EUR 2150 million in planned private leverage. Financial costs to SMEs and start-ups (compliance and application burden). Not possible to quantify.		**EU: total of EUR 425 million** (300 million for EIC Accelerator, all disbursed to 24 startups, and 125 million for InvestEU, resulting in 116 million in equity investment to 31 companies).	
Direct administrative costs	**Administrative cost related to the Chips fund**	Recurring	No administrative costs incurred.		Estimated administrative cost for SMEs and start-ups applying to and reporting under the Chips Fund, based on an average of 70 person-days (560 hours) per beneficiary for application, due diligence and reporting, valued at EUR 50-60/hour. **For 55 supported projects this yields a total cost of approx. EUR 1.7 million** (≈ EUR 30 000 per project).		**EU: approx. EUR 5.6 million**. Standard cost model combining EIC/EIF staff time and intermediaries' overheads for managing the Chips Fund. Assumes approx.160 person-days (1 280 hours) per funded project across programme design, calls, due diligence, contracting and monitoring, at EUR 80/hour. For 55 projects this gives an estimated approx. EUR 5.6 million total (≈EUR 100 000 per project, range EUR 80 000-120 000), calculated as average hours × labour cost × number of projects.	
	Administrative and Compliance burden - All Pillar I instruments	Recurring (annual)	No administrative costs incurred.		Semi-quantitative SCM estimate for application and reporting burden across all Pillar I grants (Pilot lines, competence centres, Design Platform, Quantum FPAs). Assumes on average 10-20 person-days per application: midpoint 15 days (120 hours) per participating organisation, at EUR 50/hour. Across 514 participants in 44 projects this yields **approx. EUR 3 million** in administrative and compliance costs, or approx. EUR 0.75 million per year		**EU: approx. EUR 3.1 million per year** for Pillar I under the Chips JU. **National: approx. EUR 0.7 million total** (≈EUR 0.2 million per year), assuming 25 person-days per project across national ministries and agencies.	

	Overview of costs and benefits identified in the evaluation: Pillar I							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
					over a 4-year period.			
Indirect costs	**Market distortion / Crowding-out risks**	Indirect cost	No indirect costs incurred.		Non-beneficiary firms may face competitive disadvantage; competing private investors may experience displacement of funding.		Potential resource misallocation in broader innovation ecosystem.	
	Duplication / Fragmentation risks	Indirect cost	No indirect costs incurred.		Risk of overlapping mandates for universities/RTOs and redundant investments.		National governments risk redundant investments; EU institutions risk inefficient budget allocation.	
Direct benefits	**Pilot lines established, Competence centres operational, Design platform established, SMEs/start-ups supported by Chips Fund**	Output (infrastructure)	No direct benefits identified.		Semi-quantitative: by 2025 there are 5 advanced pilot lines and around 60 SMEs/start-ups using them, plus up to 31 competence centres and 55 Chips Fund projects supported (≈EUR 62 million in grants and EUR 354 million in equity).		EU: semi-quantitative; EU funding under Pillar I has enabled 5 pilot lines and 30 competence centres, with initial monitoring showing around 60 SMEs/start-ups accessing pilot lines, roughly 100 trainees and 4 training programmes delivered through competence centres, plus 55 Chips Fund projects supported. National: semi-quantitative; participating states co-finance pilot lines with about EUR 1.86 billion in national contributions against roughly EUR 1.83 billion EU funding, and match EU support of about EUR 1 million per competence centre per year for four years in 30 centres across MS and Norway.	
	Investment leveraged (public-private)	Financial leverage	No direct benefits identified.		Semi-quantitative: the leverage ratio for the Chips Fund stands at about 5, meaning each euro of funding mobilises approximately EUR 5 from national funding and project participant investment. The Chips Fund combines EUR 300 million (EIC) and EUR 125 million (InvestEU) with expected private and EIF resources above EUR 2 billion.		EU: semi-quantitative; with a Chips JU budget of about EUR 4.175 billion and up to EUR 2.875 billion dedicated to the Initiative, a leverage ratio of 2.6 suggests that several additional billions of national and participant investment are mobilised on top of EU contributions to pilot lines, competence centres, design platform and Chips Fund. National: semi-quantitative; Member States jointly contribute around EUR 1.86 billion in co-funding to the five pilot lines and match EU support of about EUR 1 million per competence centre per year for	

	Overview of costs and benefits identified in the evaluation: Pillar I							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
								four years, while also expected to match sizeable design-platform and skills-related calls (such as the EUR 220 million grant to the design platform PCT and EUR 20 million open-source EDA call).
Indirect benefits	**Innovation and knowledge spillovers,** **Skills development and training,** **Enhanced resilience and sovereignty,** **Downstream sector benefits**	Innovation ecosystem, Human capital, Strategic/industrial policy, Competitiveness		Citizens benefit from broader innovation and economic growth. Students, engineers, technicians benefit from training opportunities. Employment prospects improved. EU citizens benefit from reduced dependency and supply chain security. Citizens benefit from improved competitiveness of EU industries (automotive, AI, defence).		Semi-quantitative: up to 60 SMEs/start-ups already use pilot lines, with certain lines expecting 40–50 SMEs per year, 20–30 prototypes and about 20 MPW runs annually; at least 100 people have completed training across 4 programmes in the competence-centre network, and newcomers account for about 41% of funded entities. SMEs/start-ups benefit from technology diffusion; large firms from supply chain synergies. Industry gains skilled workforce. Industry benefits from reduced dependency on external fabs and improved supply chain security. Downstream industries (automotive, AI, defence, IoT) benefit from improved chip supply and innovation. Productivity gains, reduced supply chain disruptions.		EU: semi-quantitative; by 2025, the EU supports 5 pilot lines, 31 competence centres and at least 4 training programmes with around 100 trainees, alongside upcoming talent-development calls worth EUR 45 million that will complement competence-centre activities. National: semi-quantitative; each Member State hosts at least one competence centre (30 centres in the EU plus Norway), with early evidence from centres such as RO_SMARTYS showing around 20 SMEs supported and 50 engineers trained, indicating potential orders of magnitude for national spillovers as centres mature.

Table 4. Pillar II CBA table

	Overview of costs and benefits identified in the evaluation: Pillar II							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
Direct financial costs	**Public subsidies for manufacturing facilities**	One-off + Recurring	No financial costs incurred.		Private investments as required to get access to State aid.		**Eleven State aid decisions for FOAK facilities: EUR 31.6 billion total** public + private investment. No EU-level financial costs incurred..	
	Investments by industry in IPCEI	One-off	No financial costs incurred.		Private investment of **EUR 13.7 billion** in IPCEI.		**IPCEI: EUR 21.8 billion** (13.7bn private + 8.1bn State aid). No EU-level financial costs incurred.	
	Operational costs of new facilities	Recurring (annual)	No financial costs incurred.		Chip manufacturers and facility operators face annual OPEX (labour, utilities, maintenance). Full operating cost data are not available yet as labour costs and energy consumption will drive costs.		No financial costs incurred	
	Administrative and compliance costs for State aid instrument	Recurring (annual)	No administrative costs incurred.		Assuming subsidised firms spend around 50 person-days per year (400 hours) on preparing and updating State aid applications, audit files and reporting, at roughly EUR 80/hour fully loaded. This gives an annual administrative and compliance cost of about **EUR 32 000 per beneficiary firm**, which for a stylised group of **30 subsidised projects** corresponds to roughly **EUR 1.0 million per year** borne by businesses.		EU: assuming about 40 person-days per project per year (320 hours) for assessing notifications, approving schemes or individual support and monitoring compliance, at an average EUR 90/hour. This implies around **EUR 28 800 per project per year**, which for **30 projects** gives an estimated **EUR 0.9 million in annual administrative cost** at EU level. National: assuming roughly 60 person-days per project per year (480 hours) for preparing and notifying aid, liaising with the Commission, issuing decisions and checking compliance, at an average EUR 80/hour. This yields about **EUR 38 400 per project per year**, or approximately **EUR 1.2 million per year** across **30 subsidised projects**, as a recurring administrative cost for Member States.	
Indirect costs	**Economic costs for**	Indirect economic	No indirect costs incurred.		Competing firms not granted FOAK recognition		EU: recognising FOAK facilities can create	

	Overview of costs and benefits identified in the evaluation: Pillar II							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
	recognition of FOAK facilities – market distortion risks	cost			face relative disadvantage. Non-recipient semiconductor firms (especially SMEs, fabless companies) and competing global players face risks from subsidy race.		indirect economic costs if support confers exclusive advantages on a small number of labelled players, distorts competition and contributes to global subsidy races, even though safeguards such as funding-gap tests and clawback mechanisms are intended to limit overcompensation and crowding out. National: FOAK recognition and large, facility-specific subsidies risk skewing investment patterns towards a few host countries, placing non-host Member States and non-recipient firms at a relative disadvantage and creating budgetary trade-offs, while fragmented national support and limited EU-level coordination can amplify subsidy-competition dynamics within the Union.	
	Opportunity costs for State aid instrument	Indirect cost	Citizens face opportunity cost of funds allocated to fabs instead of alternative social investments.		Smaller firms and RTOs may receive less support for innovation vs. large-scale manufacturing.		National governments face budgetary trade-offs (fabs vs. SMEs, R&D, or alternative sectors).	
	Environmental and infrastructure costs	Indirect cost	Local communities face environmental impact from high water, energy, and land use by new fabs.		Facility operators face high environmental compliance costs under EU standards.		National/local authorities face infrastructure upgrade costs and utility subsidy requirements.	
Direct benefits	**New manufacturing capacity created, Jobs created, Private investment mobilised, Technological upgrading**	Output (infrastructure), Employment and income, Financial leverage, Technology leadership	Local workforce benefits from high-skill jobs (construction + permanent fab employment). Citizens benefit from access to advanced technology products.		Semiconductor manufacturers and downstream industries gain new EU-based capacity from eleven FOAK facilities with total investment of EUR 32.2 billion, improving access to local production and reducing exposure to external bottlenecks. Companies benefit from an estimated 16 000 direct high-skill fab jobs and roughly 30 000		EU and MS gain strengthened industrial base. Authorities benefit from employment growth and expanded tax base. For EU and MS the eight FOAK facilities imply around 16 000 permanent high-skill jobs plus tens of thousands of construction and indirect jobs, with a direct wage bill in the order of EUR 0.9 billion per year that supports regional incomes and tax bases.	

	Overview of costs and benefits identified in the evaluation: Pillar II							
		Type	Citizens / Consumers		Businesses		Administrations (EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
					indirect jobs in suppliers and services once the FOAK pipeline is fully built out, supporting stable staffing, in-house capabilities and local supply chains. Industry gains investment opportunities. Given total FOAK investment of EUR 32.2 billion and typical aid intensities in the 30-50% range, firms are likely contributing roughly EUR 16-22 billion of private co-investment, corresponding to about 1-1.5 EUR of private funding for every Euro of public support. EU semiconductor firms gain upgraded capabilities (smaller technology nodes, advanced packaging technologies).		EU and MS demonstrate policy effectiveness through leverage ratio. Overall semiconductor investment commitments in Europe now exceeds EUR 80 billion, demonstrating a strong multiplier effect of State aid. For EU and MS the concentration of investment in advanced nodes, wide-bandgap power electronics, packaging and photonics strengthens Europe's technological capabilities beyond mature processes and supports long-term competitiveness and sovereignty in critical semiconductor value chains.	
Indirect benefits	**Resilience of EU supply chains, Increased global competitiveness, Regional development and clustering, Knowledge transfer and spillovers**	Strategic/industrial policy Industrial policy outcome Regional cohesion Innovation ecosystem	EU citizens benefit from supply chain security and reduced vulnerability to global shocks. Citizens benefit from stronger EU industrial position globally. Local communities benefit from spillover economic growth in semiconductor clusters (e.g., Dresden, Crolles). Citizens benefit from broader innovation ecosystem strengthening.		Industry faces lower risk from global shocks; downstream sectors gain stable chip access. EU semiconductor firms gain improved market position vs. US/Asia competitors. Investors/shareholders benefit from returns. Benchmark of EU vs global fabs in cost, yield, capacity, process node. SMEs in supply chain benefit from supplier contracts and partnerships. SMEs/start-ups gain access to advanced technology through collaborations. Number of joint projects with RTOs/universities, patents/publications co-authored, SME collaborations.		EU and MS gain supply chain security.	

Table 5. Pillar III CBA table

	Overview of costs and benefits identified in the evaluation: Pillar III							
		Type	Citizens / Consumers		Businesses		(EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
Direct financial costs	**Priority-rated orders**	Contingent (if crisis activated)	No financial costs incurred		Semiconductor manufacturers must comply with priority orders, facing loss of revenue from deprioritised customers, production disruptions, foregone contracts, strained business relations. These are opportunity costs. Downstream customers not prioritised may face delays or shortages if crisis stage declared.		No actual costs incurred yet.	
Direct administrative costs	**Monitoring mechanism costs**	Recurring (annual)	No administrative costs incurred.		Assuming around 50 key semiconductor firms are regularly surveyed, each spending roughly 160 hours per year (about 20 person-days) collecting and reporting supply-chain data at EUR 70/hour, the annual compliance cost of the monitoring mechanism for industry is about **EUR 0.6 million in total** (≈EUR 11 000-12 000 per firm).		EU: If around 8 dedicated FTEs across DG CNECT and the ESB work on monitoring at an average fully loaded cost of EUR 120 000 per year, complemented by roughly EUR 0.5 million in analytical support contracts, the annual EU-level monitoring cost is around **EUR 1.5 million**. National: Assuming in each of the 27 MS about 0.5 FTE (≈800 hours a year) in relevant ministries and agencies is devoted to data provision at EUR 70/hour, the annual national administrative cost of feeding the EU monitoring mechanism is roughly EUR 1.5 million in total, or about **EUR 55 000 per MS**.	
	Crisis coordination costs	Recurring (annual)	No administrative costs incurred.		Industry faces costs of engagement in consultations and compliance with crisis protocols (when activated).		EU and MS face coordination costs, administrative participation, reallocation of staff. Costs have been minimal to date as no crisis stage declared.	

	Overview of costs and benefits identified in the evaluation: Pillar III							
		Type	Citizens / Consumers		Businesses		(EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
	Export restrictions and information obligations	Contingent (if crisis activated)	EU trading partners may impose retaliatory measures if export controls activated.		Semiconductor manufacturers face restricted market access and compliance costs. Exporters in downstream industries face delays and trade disruptions. Lost export revenues, potential retaliation from trade partners.		No actual costs incurred yet. These are contingent costs that would only materialise if crisis stage declared and export restrictions implemented.	
	Legal and enforcement costs	Contingent (if crisis activated)	No administrative costs incurred.		No administrative costs incurred.		EU (DG COMP involvement) and national authorities (customs, regulators, trade ministries) face legal enforcement costs if crisis measures implemented. Costs minimal to date.	
Indirect costs	**Indirect costs**	n/a	No indirect costs incurred.		No indirect costs incurred.		No indirect costs incurred.	
Direct benefits	**Supply chain monitoring mechanism established, Crisis coordination framework in place, Early warning of disruptions**	Output (systemic visibility) Output (institutional preparedness) Risk mitigation	No direct benefits identified.		Industry benefits from predictability and reduced uncertainty through supply/demand trend visibility. Industry benefits from predictable crisis management protocols and clearer roles. Industry gains ability to adjust production planning. Downstream sectors benefit from early risk awareness through monitoring and reporting obligations.		EU and MS gain better evidence base for policymaking decisions. EU institutions gain coordination capacity; national authorities have clearer roles in crisis response.	
Indirect benefits	**Faster crisis response capacity, Improved resilience of EU supply chains, Strengthened EU global position**	Contingent (if crisis activated) Strategic/industrial policy Geopolitical influence	EU citizens would benefit from continuity of supply for essential products if crisis stage activated and measures effective. Society at large benefits from reliable supply of critical products through structural risk management. Citizens benefit indirectly from		Critical downstream industries (from the critical sectors, including , defence, health) would benefit from reduced disruption severity/duration through priority-rated orders and export restrictions if triggered. Industry benefits from reduced vulnerability to supply shocks through structural risk management mechanisms.		These benefits remain contingent on formal declaration of semiconductor crisis stage. As no such crisis has occurred to date, these benefits have not yet materialised. EU institutions and MS gain enhanced resilience capacity. EU institutions gain strategic autonomy in crisis governance of semiconductors. Global partners benefit from predictability of EU response.	

	Overview of costs and benefits identified in the evaluation: Pillar III							
		Type	Citizens / Consumers		Businesses		(EU and national)	
			Quantitative	Comment	Quantitative	Comment	Quantitative	Comment
			enhanced EU strategic autonomy.					